SGS-THOMSON MICROELECTRONICS

STG 2000 rev. C

MULTIMEDIA ACCELERATOR

PRELIMINARY INFORMATION

KEY FEATURES

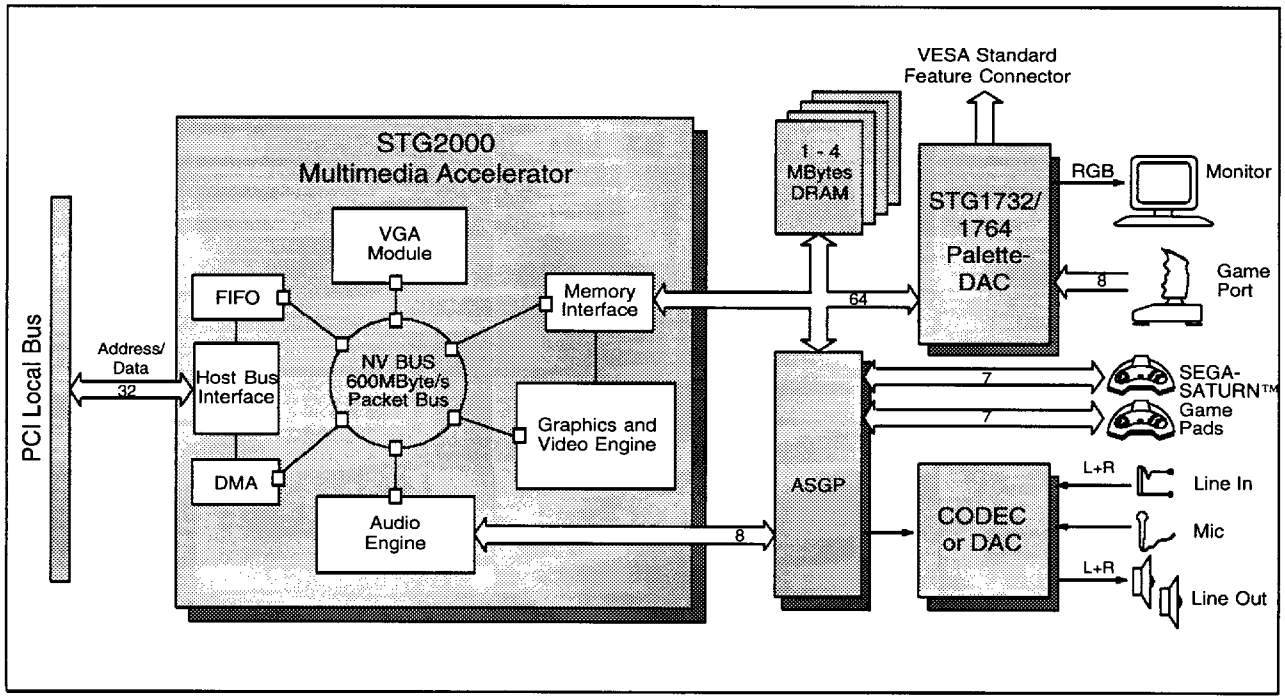
- Single-chip Multimedia Accelerator
- Support for Industry Standards
  - Acceleration for all DirectX API's under Windows 95
  - Industry-leading GUI Acceleration
  - Full-Motion Video Acceleration (Indeo, MPEG, Cinepak)
- Real-Time Texture Mapped 3D Graphics
- Accelerates All 3D Standards: triangles, quadrilaterals and curves
- Hardware Audio WaveTable Synthesis
- Enhanced Digital Game Port
- System level performance and cost optimization

Designed for Microsoft Windows'95

DESCRIPTION

The STG2000 chip from SGS-THOMSON is the PC industry's first single chip accelerator supporting all of the multimedia features supported under Windows 95. These features include: 2D/GUI acceleration, real time texture mapped 3D acceleration, Wavetable Audio acceleration, Full Motion Video acceleration, and Digital Input acceleration, in short, acceleration of all of the key DirectX API's supported under Windows 95. The STG2000 also provides support for legacy applications with full multimedia drivers for Windows 3.11 and an integrated VGA for DOS.

BLOCK DIAGRAM



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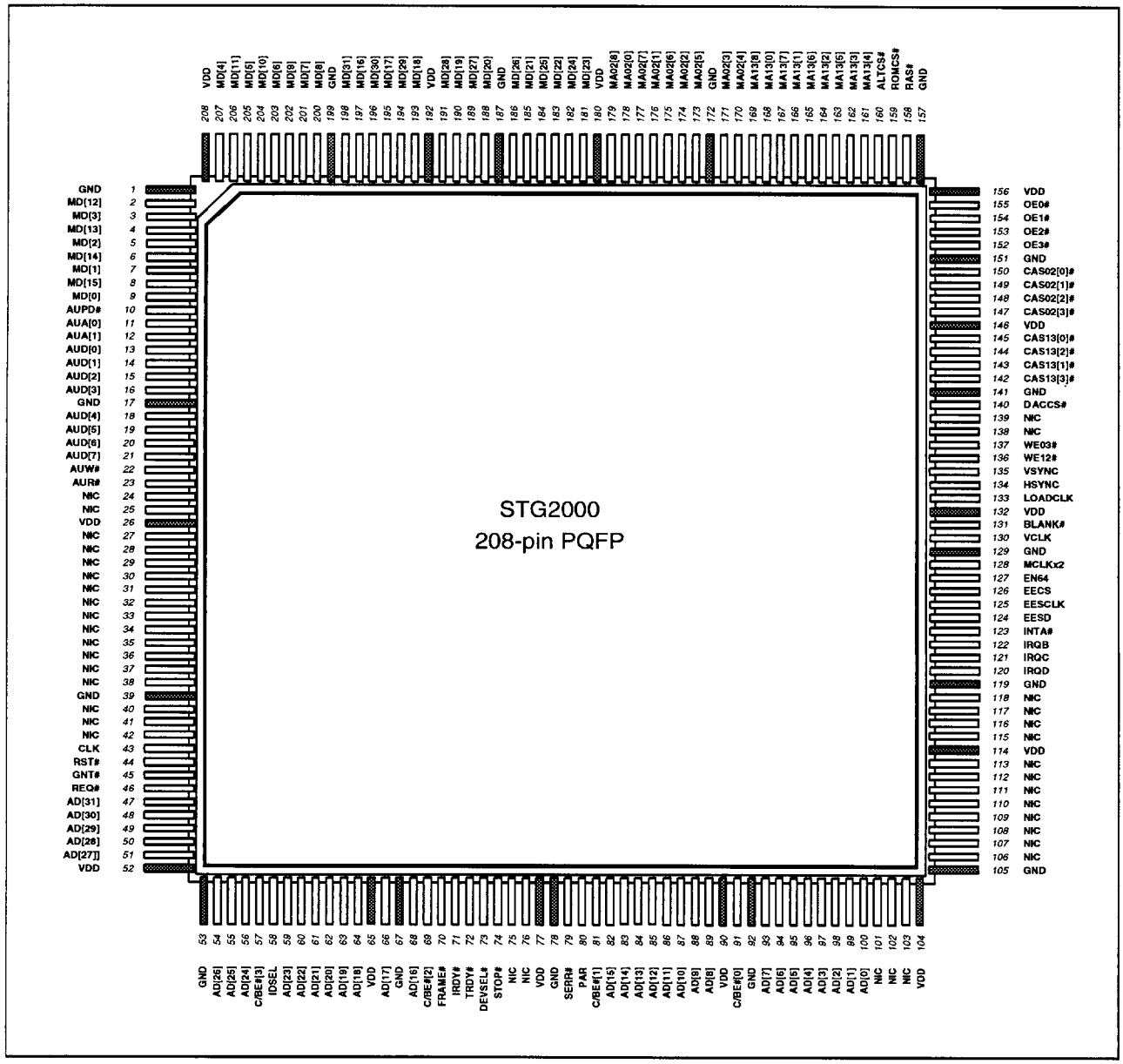
1 DEVICE PINOUTS

Power and ground pins are denoted by shading in the following diagram.

1.1 STG2000 PCI DRAM PIN-OUT



NOTES

1 NIC = No Internal Connection. Do not connect to these pins.

2 VDD=3.3V

2 PIN DESCRIPTIONS

2.1 PCI BUS INTERFACE

Signal	I/O	Description
CLK	I	PCI clock. This signal provides timing for all transactions on the PCI bus, except for **RST#** and **INTA#**. All PCI signals are sampled on the rising edge of **CLK** and all timing parameters are defined with respect to this edge.
RST#	I	PCI reset. This signal is used to bring PCI-specific registers, sequencers and signals to a consistent state. When **RST#** is asserted all PCI output signals are tristated.
AD[31:0]	I/O	32-bit multiplexed address and data bus. A bus transaction consists of an address phase followed by one or more data phases.
C/BE[3:0]#	I/O	Multiplexed bus command and byte enable signals. During the address phase of a transaction **C/BE[3:0]#** define the bus command, during the data phase **C/BE[3:0]#** are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes contain valid data. **C/BE[0]#** applies to byte 0 (LSB) and **C/BE[3]#** applies to byte 3 (MSB).
PAR	I/O	Parity. This signal is the even parity bit generated across **AD[31:0]** and **C/BE[3:0]#**. **PAR** is stable and valid one clock after the address phase. For data phases **PAR** is stable and valid one clock after either **IRDY#** is asserted on a write transaction or **TRDY#** is asserted on a read transaction. Once **PAR** is valid, it remains valid until one clock after completion of the current data phase. The master drives **PAR** for address and write data phases; the target drives **PAR** for read data phases.
FRAME#	I/O	Cycle frame. This signal is driven by the current master to indicate the beginning of an access and its duration. **FRAME#** is asserted to indicate that a bus transaction is beginning. Data transfers continue while **FRAME#** is asserted. When **FRAME#** is deasserted, the transaction is in the final data phase.
IRDY#	I/O	Initiator ready. This signal indicates the initiator's (bus master's) ability to complete the current data phase of the transaction. **IRDY#** is used in conjunction with **TRDY#**. A data phase is completed on any clock when both **IRDY#** and **TRDY#** are sampled as being asserted. During a write, **IRDY#** indicates that valid data is present on **AD[31:0]**. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both **IRDY#** and **TRDY#** are asserted together.
TRDY#	I/O	Target ready. This signal indicates the target's (selected device's) ability to complete the current data phase of the transaction. **TRDY#** is used in conjunction with **IRDY#**. A data phase is completed on any clock when both **TRDY#** and **IRDY#** are sampled as being asserted. During a read, **TRDY#** indicates that valid data is present on **AD[31:0]**. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both **IRDY#** and **TRDY#** are asserted together.
STOP#	I/O	**STOP#** indicates that the current target is requesting the master to terminate the current transaction.
IDSEL	I	Initialization device select. This signal is used as a chip select during configuration read and write transactions.
DEVSEL#	I/O	Device select. When acting as an output **DEVSEL#** indicates that the STG2000 has decoded the PCI address and is claiming the current access as the target. As an input **DEVSEL#** indicates whether any other device on the bus has been selected.
REQ#	O	Request. This signal is asserted by the STG2000 to indicate to the arbiter that it desires to become master of the bus.
GNT#	I	Grant. This signal indicates to the STG2000 that access to the bus has been granted and it can now become bus master.

Signal	I/O	Description
SERR#	O	System error. This signal is used by the STG2000 to report parity errors and significant system errors. **SERR#** is pure open drain and is actively driven for a single PCI clock, the assertion of **SERR#** being synchronous to that clock.
INTA#	O	Interrupt request line. This open drain output is asserted and deasserted asynchronously to **CLK**.
IRQB, IRQC, IRQD	O	Interrupt Request Lines. These interrupt signals are active high, level triggered interrupts that may be connected to the IRQ lines on the ISA bus.

2.2 DRAM MEMORY INTERFACE

Signal	I/O	Description
MD[31:0]	I/O	The 32-bit memory data bus. **MD[31:0]** are also used to load pixel data into the Palette-DAC, **MD[7:0]** to access the 8-bit EPROM, **MD[15:8]** to access the Palette-DAC and **MD[30:16]** to address the 32KByte EPROM.
MA02[8:0]	O	Memory Address bus for DRAM banks 0 and 2. Supports symmetric address 256K x n memory architectures.
MA13[8:0]	O	Memory Address bus for DRAM banks 1 and 3. Supports symmetric address 256K x n memory architectures.
RAS#	O	Row Address Strobe for all memory banks.
CAS02[3:0]#	O	Column Address Strobe for each byte in DRAM banks 0 and 2.
CAS13[3:0]#	O	Column Address Strobe for each byte in DRAM banks 1 and 3.
WE03#	O	Write Enable for DRAM banks 0 and 3.
WE12#	O	Write Enable for DRAM banks 1 and 2.
OE0#, OE1#, OE2#, OE3#	O	Output Enable for each DRAM bank.
EN64	O	This output is used in 2 and 4MByte framestores which interface to the STG1764. When high this pin tri-states external bus transceivers between two 32-bit interfaces to the 64-bit Pixel Port of the STG1764. When low this pin enables the connection between the two 32-bit interfaces.
MCLKx2	I	Memory Clock x 2. This signal provides a timing reference to all internal functions of the STG2000. This clock is sourced from the STG1732/64 memory clock output. **MCLKx2** runs at twice the frequency of the internal memory clock.

2.3 EEPROM INTERFACE

Signal	I/O	Description
EECS	O	EEPROM chip select. This signal requires an external 50KΩ pull-down to hold the EEPROM in a quiescent state during reset.
EESD	I/O	EEPROM bidirectional data.
EESCLK	O	EEPROM Clock. Data is clocked into/out of the 93C46A based on the rising edge of this clock as defined by the Microwire protocol.

2.4 DISPLAY INTERFACE

Signal	I/O	Description
DACCS#	O	Enables the Palette-DAC to be accessed via the data bus. This pin is used in conjunction with **MD[31:0]** to load pixel data and **MD[15:8]** to access the Palette-DAC register.
LOADCLK	O	Connects to the Palette-DAC **LOADCLK** pin. The rising edge of this signal controls sampling on the Palette-DAC **LOADEN#** and pixel input pins.
BLANK#	O	Blanking signal sampled by the Palette-DAC on the rising edge of **VCLK**. A '0' sampled will, after a pipeline delay, turn the DAC outputs off. A special protocol on the Palette-DAC **BLANK#** and **VCLK** pins enables the controller to reset various functions of the Palette-DAC at the start of frame flyback.
VCLK	I	Video Clock. This clock is sourced from the Palette-DAC memory clock output. The **VCLK** frequency is the video frequency at the DACs divided by 1, 2, 4, 8, or 16, depending on the selected mode.
VSYNC	O	Vertical sync supplied to the display monitor. No buffering is required to drive a local monitor.
HSYNC	O	Horizontal sync supplied to the display monitor. No buffering is required to drive a local monitor.

2.5 AUDIO CODEC INTERFACE

Signal	I/O	Description
AUW#	O	Audio Write command strobe.
AUR#	O	Audio Read command strobe.
AUA[1:0]	O	Audio Address outputs.
AUD[7:0]	I/O	Audio Data bus. These pins transfer data and control information between the Audio Codec and the STG2000.
AUPD#	O	Places the Audio Codec in its low power consumption mode.

2.6 DEVICE ENABLE SIGNALS

Signal	I/O	Description
ROMCS#	O	Enables reads from an external 32Kx8 EPROM or Flash ROM. This signal is used in conjunction with **MD[7:0]** for the ROM data bus, **MD[30:16]** for the 15-bit address, and **MD[31]** for the R/W# select.
ALTCS#	O	Allows an 8-bit external device with up to 32KBytes of address space to be accessed via the memory data bus. This signal is used in conjunction with **MD[7:0]** for an 8-bit data bus, **MD[30:16]** for the 15-bit address bus, and **MD[31]** for the R/W# select.

3 OVERVIEW OF THE STG2000

3.1 SINGLE-CHIP ACCELERATOR FOR ALL OF WINDOWS 95

The STG2000 chip from SGS-THOMSON Microelectronics is the PC industry's first single chip accelerator supporting all of the multimedia features supported under Windows 95. These features include: 2D/GUI acceleration, real time texture mapped 3D acceleration, Wavetable Audio acceleration, Full Motion Video acceleration, and Digital Input acceleration, in short, acceleration of all of the key DirectX API's supported under Windows 95. The STG2000 also provides support for legacy applications with full multimedia drivers for Windows 3.11 and an integrated VGA for DOS.

This concurrent acceleration is achieved through individual hardware engines within the chip connected by a 600MByte/s data bus. These hardware engines provide functionality that would have required 3 separate PC cards in the past. Combining the engines in one chip not only eliminated the cost of the multiple cards, more importantly, it enabled resources to be optimized at a system level among the separate engines. A total of 1MByte of framebuffer memory is all that is required to obtain high performance with all of the concurrent engines. The rest of the required resources such as texture memory and audio wave samples, are DMA'd from system memory using the on chip bus mastering DMA engine.

The combination of single chip solution and high performance using minimal memory results in the lowest cost yet highest performance Windows 95 accelerator in the market today.

Goals: Better, Faster, Lower Cost, Accelerate Today's Standards

The design goals for the STG2000 chip were to create a complete multimedia solution that was: lower cost, higher performance, greater functionality and yet capable of being a drop-in replacement for today's standard GUI accelerators. As such, all of the functionality in today's graphics accelerator chips are included in the STG2000. However the STG2000 is unique in that all of the other key components in today's Interactive Multimedia PC have also been incorporated into the same chip. This means that functionality such as real-time texture mapped 3D graphics, Wavetable Audio, Digital Gameport, and Full Motion Video Acceleration, are all concurrently hardware accelerated on a single piece of silicon. This integration of functionality permits highly efficient allocation of system resources so that a single megabyte of framebuffer memory can be shared among all of the hardware engines on the chip thereby ensuring low cost. This encapsulated multimedia subsystem functionality enables STG2000 to be the industry's first complete DirectX accelerator, accelerating all the pieces of Microsoft's DirectX API's. The STG2000 chip provides breakthrough levels of functionality, performance, low cost, and differentiation for the PC marketplace.

KEY Features

- Single-chip Multimedia Accelerator
- Support for Industry Standards
  - Acceleration for all DirectX API's under Windows 95
  - Industry-leading GUI Acceleration
  - Full-Motion Video Acceleration (Indeo, MPEG, Cinepak)
- Real-Time Texture Mapped 3D Graphics
- Accelerates All 3D Standards: triangles, quadrilaterals and curves
- Hardware Audio WaveTable Synthesis
- Enhanced Digital Game Port
- System level performance and cost optimization

3.2 STANDARDS ACCELERATION

Direct-X Acceleration Under Windows 95

The STG2000 chip incorporates functionality that directly accelerates today's leading API standard, Microsoft's Windows 95 DirectX API's. It is currently the only device on the market today that can concurrently hardware accelerate DirectDraw, DirectVideo, Direct3D, DirectSound, and DirectInput. As content developers migrate to this set of API standards, STG2000 designs will be poised to provide the complete acceleration solution.

- DirectDraw/DirectVideo - Hardware 2D/GUI/Video engine
- Direct3D - Hardware real time 3D texture mapping engine
- DirectSound - Hardware digital mixing - no CPU overhead
- DirectInput - Digital Gameport - supports standard PC joysticks and SEGA™ peripherals

GUI Acceleration Under Windows 95

- Extensive support for Microsoft's DirectDraw API
- Optimized for multiple color depths including 8, 15, 24, and 30 bits per pixel
- Hardware color dithering - higher quality with less framebuffer usage

Full-Motion Video Acceleration

The STG2000 graphics engine accelerates full-motion video playback and can sustain 30 frames per second of true-color digital video. Hardware video acceleration provides image enhancement and scaling of video streams to full-screen display.

- Support for DirectVideo in Windows 95
- Video interpolation for enhanced image quality
- Integration of graphics and video enabling special effects
- Accelerated playback of industry standard CODECs such as MPEG, Indeo, and Cinepak
- Interframing for reduced flicker

3.3 REAL TIME TEXTURE MAPPED 3D GRAPHICS

The STG2000's 3D Graphics engine was architected from inception for consumer interactive multimedia. The resulting price goals drove the design of a graphics engine that maintains its high performance with minimal framebuffer memory requirements. The STG2000 is able to maintain its high performance in only 1MByte of framebuffer memory.

Consumer multimedia also dictated that the STG2000 was designed to accelerate consumer style 3D graphics. It's optimization focuses on delivering the highest possible frame rate for the maximum in interactivity. This optimization is evident on games like Virtua Fighter Remix™, which is a 640x400, 16 bits per pixel game that runs at greater than 30 frames per second. To put it in perspective, on today's 133MHz Pentiums without acceleration, it is only possible to run similar games at 320x200, 8 bits per pixel at 20fps.

Some key capabilities of the 3D engine are:

- High performance acceleration of perspective-correct textured triangles, quadrilaterals, and curves
- Highest rendering pixel rate for fastest 3D frame rate
- Photorealistic 3D texture mapping, including lighting, fog, transparency, etc.
- Video Texturing - ability to treat video as a texture. Allows user to map video onto 3D objects.

3.4 HARDWARE AUDIO WAVETABLE SYNTHESIS ENGINE

The STG2000 chip integrates a high performance audio engine to deliver the highest fidelity and realism for today's interactive multimedia applications. With support for dynamic downloadable samples, developers can utilize custom samples for exciting sound and MIDI effects. Additionally, the NV Architecture's native synchronization capability allows developers to precisely control the relationship of audio playback to 3D graphics, video, or other audio streams. This capability is necessary for a truly interactive experience.

For the system integrator, the STG2000's audio solution allows multiple options on how to implement the audio subsystem. These options offer solutions at various pricepoints and integration levels depending on which of the possible audio interfaces is desired.

- Support for industry audio standards:
  - Windows 95 DirectSound API
  - MPU-401, General MIDI, Miles Audio Interface Library (AIL), HMI Sound Operating System (SOS)
- Hardware 350MIPS Audio Engine supporting 32 channels of 16-bit wavetable sound
- Concurrent playback and hardware mixing of up to 50 channels of digital audio
- Downloadable Wavetable samples stored in system memory instead of dedicated ROM/RAM
- Support for effects such as tremolo, vibrato and portamento
- Support for industry standard I^2S interface

3.5 DIGITAL GAMEPORT ENGINE

The STG2000 is the first product to feature an IBM compatible digital game port as well as two SEGA-SATURN™ peripheral ports. Where standard game ports demand the near-constant intervention of the PC's microprocessor, STG2000's digital game port DMA-bursts the joystick's position without interrupting the processor. The benefit is better overall system performance, a crucial advantage in multimedia applications. The STG2000 game

port also provides higher resolution and sampling rates than standard game ports, enabling a finer degree of joystick control and quicker response to user actions.

Another key advantage of the digital gameport is that it allows a multitude of accessories and functionality not possible on the PC before. Two players can now simultaneously compete using the 2 SEGA™ ports available on every STG2000 card. Up to six players can concurrently participate in multiplayer titles using the optional multi-tap device also supported by this port.

- All gaming ports are supported in Microsoft's DirectInput API
- 8-channel digital game port with advanced analog/digital sampler
- 13-bit capture resolution with sample rates up to 92Hz (versus a typical game port of 8-bit resolution and 1Hz sample rate)
- Support for SEGASATURN™ peripherals
- Bus mastering DMA frees up to 12% of a Pentium class CPU's bandwidth

3.6 HIGHEST OVERALL SUBSYSTEM PERFORMANCE

The STG2000 chip was not designed as a single independent entity. The surrounding components were all taken into account in the performance optimizations that took place. This concept of system performance vs. single chip performance, has always been practiced in the game console industry. That industry has always realized that it is no good just having great graphics, if audio or gameport or video holds back the final application's performance. That is the main reason why PC titles were never capable of achieving the quality of the top 3D console box titles.

Until now, the solutions in the PC industry have always been fragmented and independent. The software developer, for example, had no idea what Sound card is coupled with which 3D card, and therefore has always had to program to the lowest common denominator, sacrificing overall frame rate and title quality.

The STG2000 is the PC industry's first self contained multimedia subsystem. Knowing the performance of all available components ensures consistently high performance throughout the entire subsystem. This allows the STG2000 to power the leading titles with the highest possible frame rates.

3.7 LOWEST OVERALL SUBSYSTEM COST

There are usually two main components in the cost of a multimedia subsystem. The cost of the media accelerator chips themselves, and the cost of the memory associated with the individual media accelerators. By integrating the key media types into a single chip, SGS-THOMSON Microelectronics allows the board/system integrator to provide the full consumer interactive multimedia experience in a single low cost card.

Perhaps more importantly, the integration of the various media accelerators allowed for system level optimization of memory resources. Traditionally, the 2D card would have required frame buffer memory (1-2MByte), the 3D card requires Z buffer, and texture memory (2-4MByte) and the Audio card requires even more memory for storing wavetable samples (1-4MByte).

In the STG2000 subsystem, only 1MByte of frame-buffer memory is necessary to support the combination of 2D, Video, 3D, and Wavetable Audio. The unique hardware architecture combined with PCI bus mastering DMA capabilities allows the STG2000 chip to store wavetable samples, and 3D texture maps in system memory, resulting in the lowest possible memory requirements. This combination of chip integration and memory integration results in the lowest overall system cost.

3.8 SCREEN RESOLUTIONS

Screen resolutions and refresh rates supported by the STG1764 135MHz 64-bit Palette-DAC with 2MBytes of DRAM include:

Pixel depth	Resolutions and refresh rate supported				
	640× 480	800× 600	1024× 768	1152× 864	1280× 1024
8	96Hz	96Hz	96Hz	96Hz	75Hz
15	96Hz	96Hz	75Hz	70Hz	
24/30	96Hz	75Hz			

3.9 ADVANCED SEMICONDUCTOR PROCESS

The STG2000 is manufactured on SGS-THOMSON's advanced 0.5 micron, 3 layer metal, 3.3V process with SURE 6 quality and reliability standards. The low power dissipation and reduced output switching noise significantly increases system reliability. Output drivers are 5V-tolerant process compensated for PCI compatibility.

3.10 HIGH-PERFORMANCE MULTIMEDIA SUBSYSTEM

The STG2000 Multimedia Accelerator brings together an unrivaled level of multimedia functionality which previously required dozens of components and multiple PCBs. Typical parts count for 1 and 2MByte DRAM implementations includes the following active components:

Active component	1MByte	2MByte
STG2000 Multimedia Accelerator	1	1
STG1764 Palette-DAC	1	1
SEGA™ interface ASIC	1	1
256Kx16	2	4
Audio DAC	1	1
EPROM	1	1
EEPROM	1	1
Dual Op-Amp	2	2
Total	**10**	**12**

3.11 REFERENCE DESIGN KIT

A Reference Design Kit (RDK) is available for the STG2000. This includes all necessary information required to design and manufacture a family of high performance PC Multimedia Accelerator Cards based on the STG2000 with different memory options.

The RDK includes:

- STG2000 and STG1764 Palette-DAC Databook
- A detailed DESIGN GUIDE
  - Options for using SoundBlaster™ compatible CODECs
  - 1 and 2MBytes DRAM board design and schematics
  - Bill of Materials and a device cross reference
- Gerber/Aperture/Drill files for turnkey board production
- BIOS, BIOS modification utilities, device drivers, and diagnostics

3.12 SOFTWARE DEVELOPMENT KIT

A Software Development Kit (SDK) (which includes header files, sample code, manuals, and on-line documentation) is available for Developers taking advantage of the capabilities of NV Architecture or using NVLIB.

4 HOST BUS INTERFACES

4.1 PCI BUS INTERFACE

PCI capability

The STG2000 supports a glueless interface to PCI (2.0) with both master and slave capabilities. The host interface is fully compliant with the 32-bit PCI (2.0) specification.

The Multimedia Accelerator supports operation up to 33MHz with zero-wait state capability for bursts exceeding 128 bytes and full bus mastering capability handling 32-byte burst reads and 16-byte burst writes.

Figure 1. PCI interface pin connections

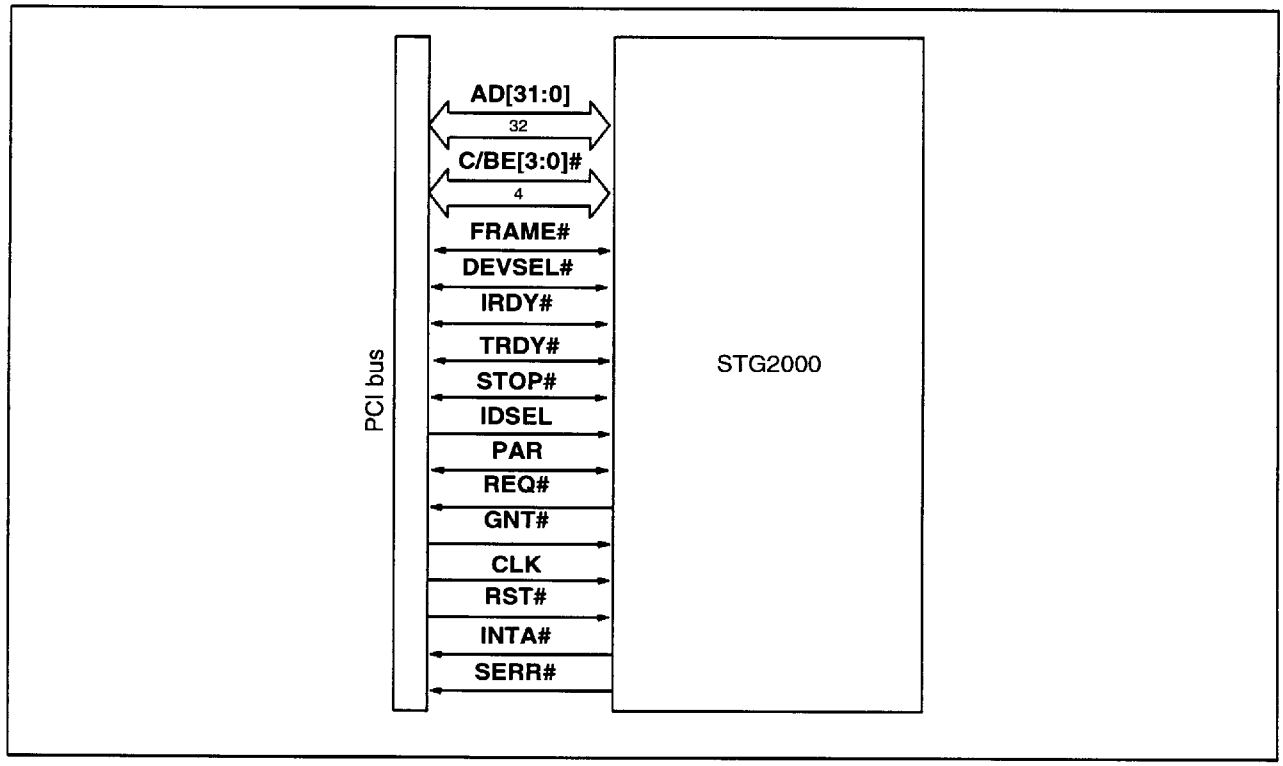


Table 1. PCI bus commands supported by the STG2000

Bus master	Bus slave
Memory read and write	Memory read and write
Memory read line	I/O read and write
	Configuration read and write
	Memory read multiple
	Memory read line
	Memory write invalidate

PCI timing parameters

The timing specification of the PCI interface takes the form of generic setup, hold and delay times of transitions to and from the rising edge of **CLK** as shown in Figure 2.

Figure 2. PCI timing parameters

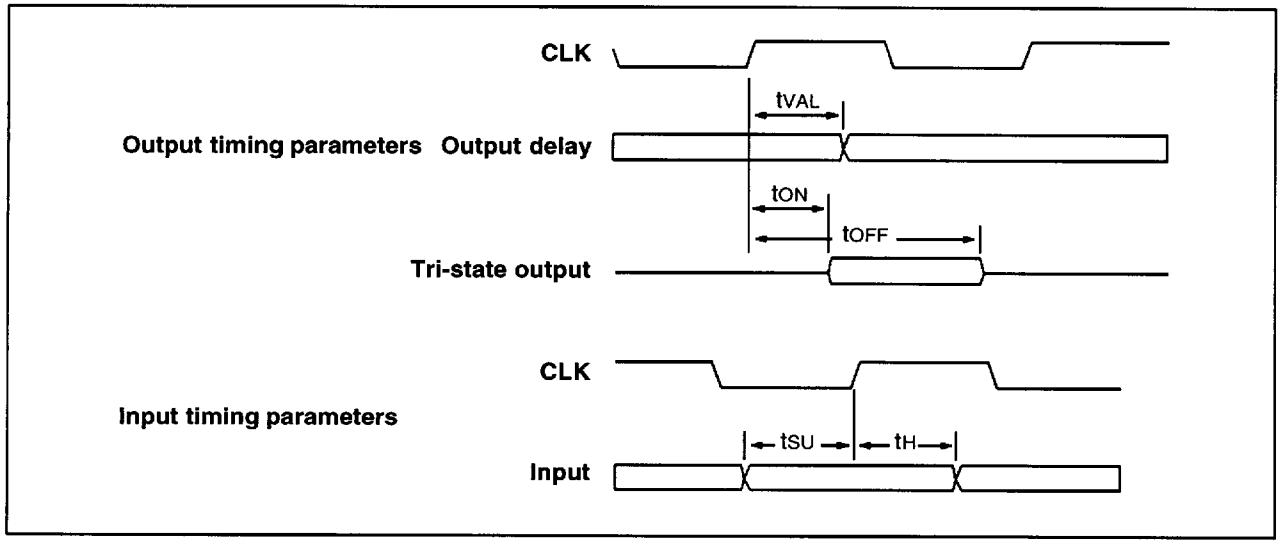


Table 2. PCI timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tVAL	**CLK** to signal valid delay (bussed signals)	2	11	ns	1
tVAL(PTP)	**CLK** to signal valid delay (point to point)	2	12	ns	1
tON	Float to active delay	2		ns	
tOFF	Active to float delay		28	ns	
tSU	Input set up time to **CLK** (bussed signals)	7		ns	1
tSU(PTP)	Input set up time to **CLK** (**GNT#**)	10		ns	1
tH	Input hold time from **CLK**	0		ns	

NOTE

1 **REQ#** and **GNT#** are point to point signals and have different valid delay and input setup times than bussed signals. All other signals are bussed.

Figure 3. PCI Target write - Slave Write (single 32-bit with 1-cycle **DEVSEL#** response)

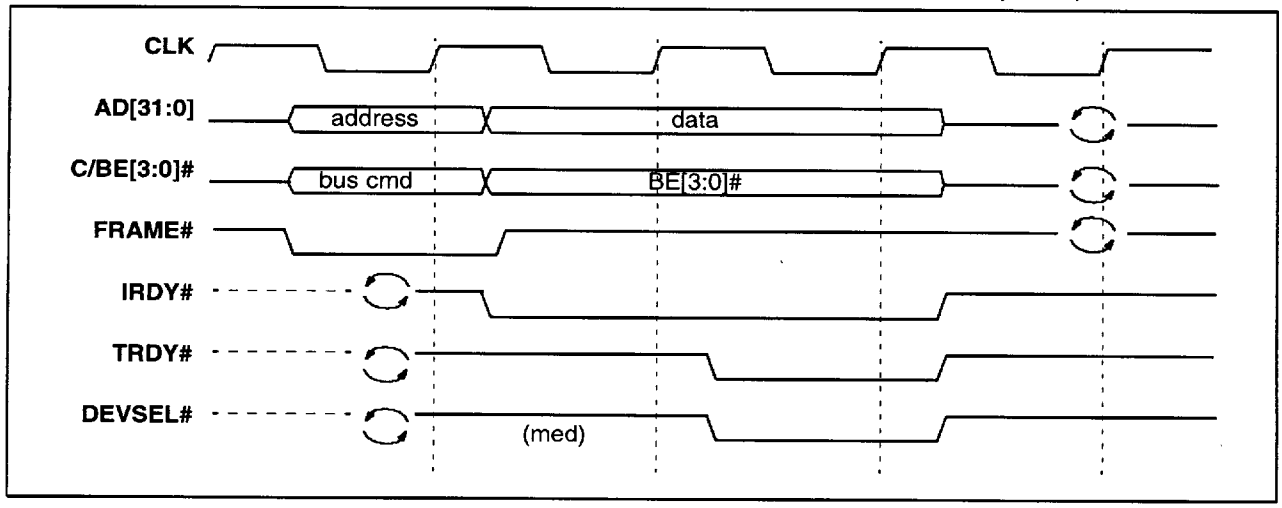


Figure 4. PCI Target write - Slave Write (multiple 32-bit with zero wait state **DEVSEL#** response)

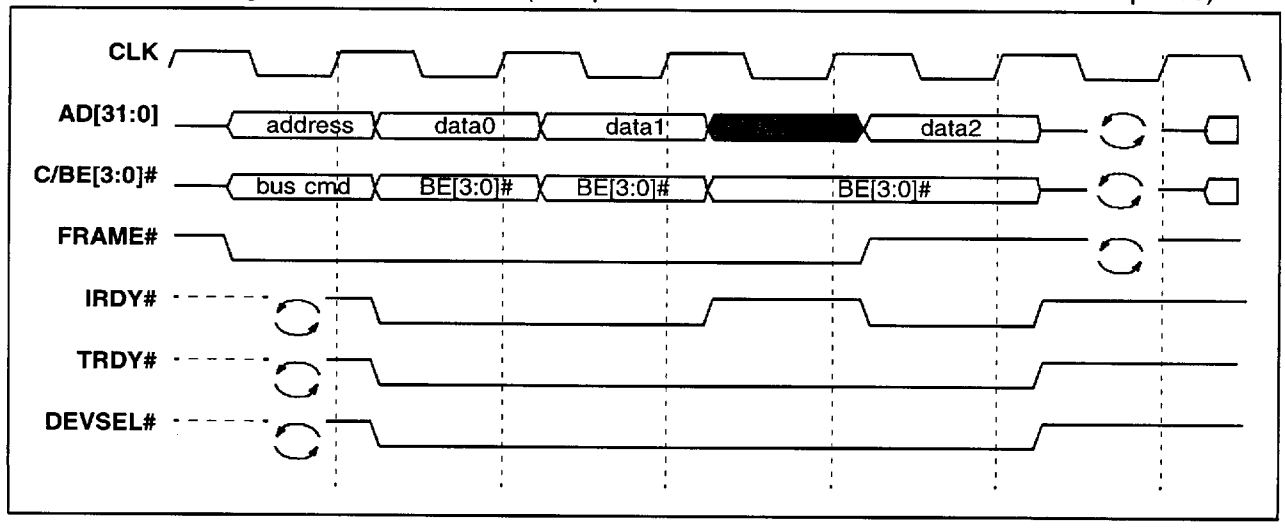


Figure 5. PCI Target read - Slave Read (1-cycle single word read)

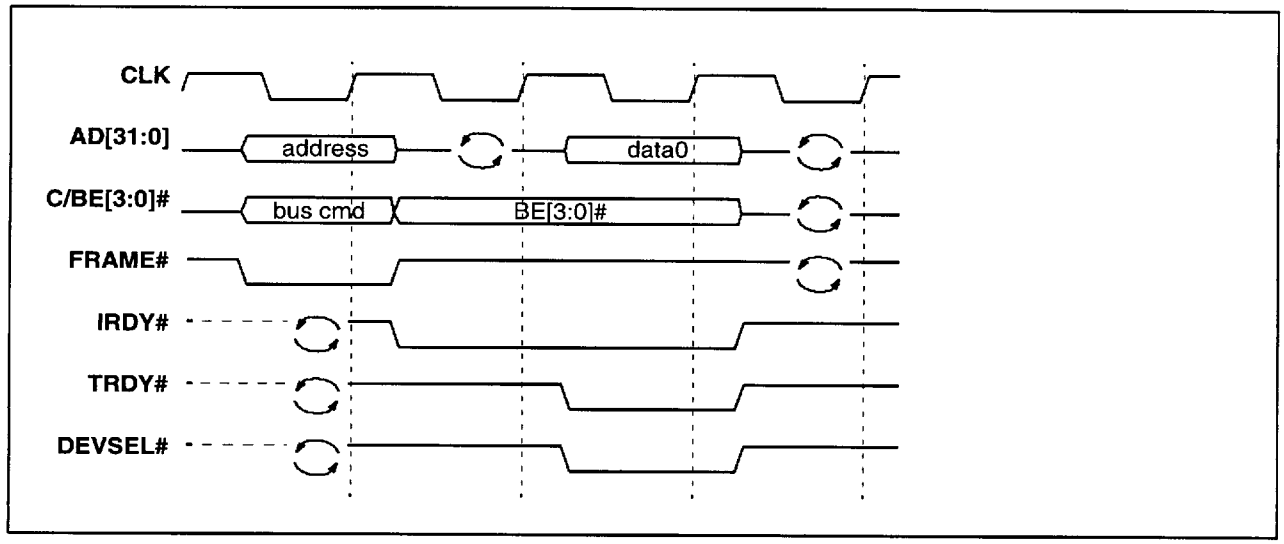


Figure 6. PCI Target read - Slave Read (slow single word read)

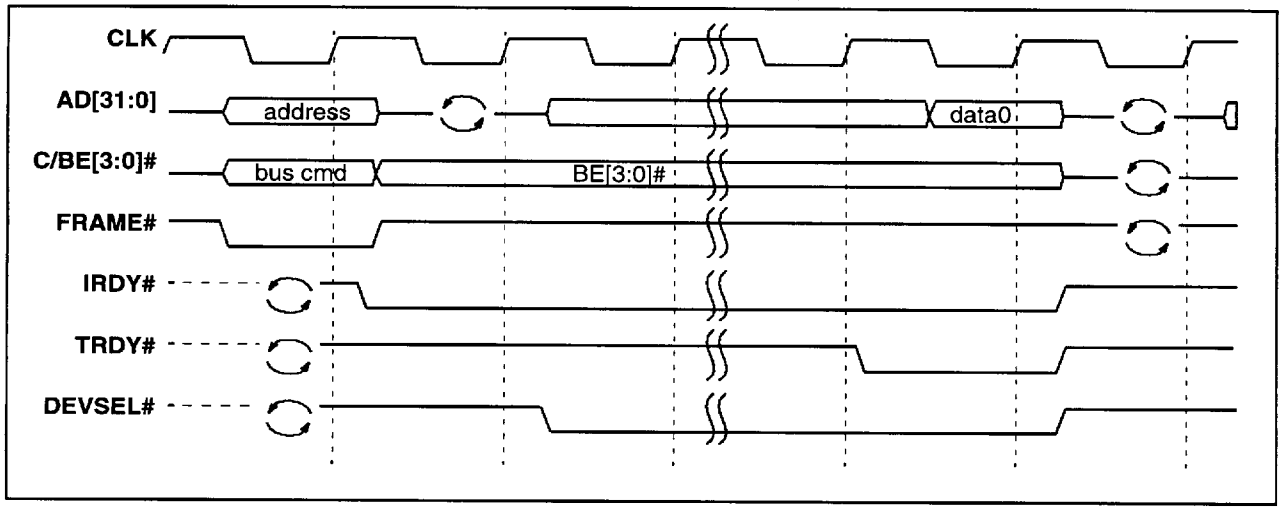


Figure 7. PCI Master write - multiple word

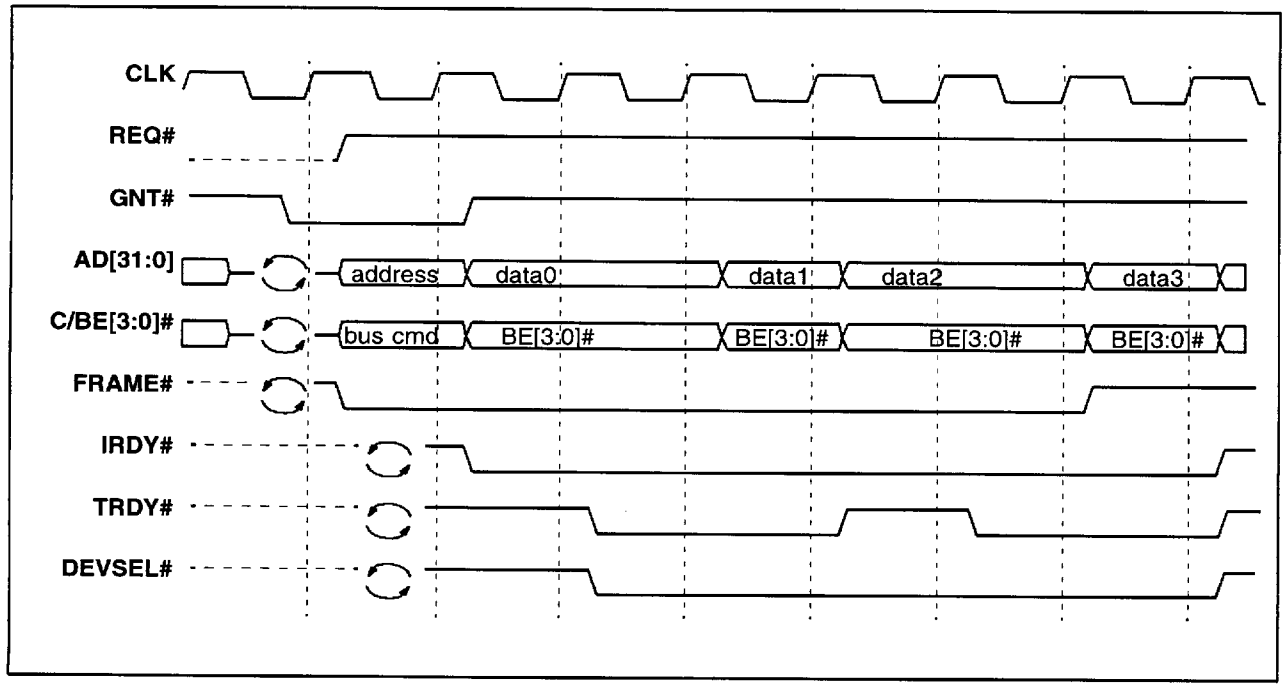
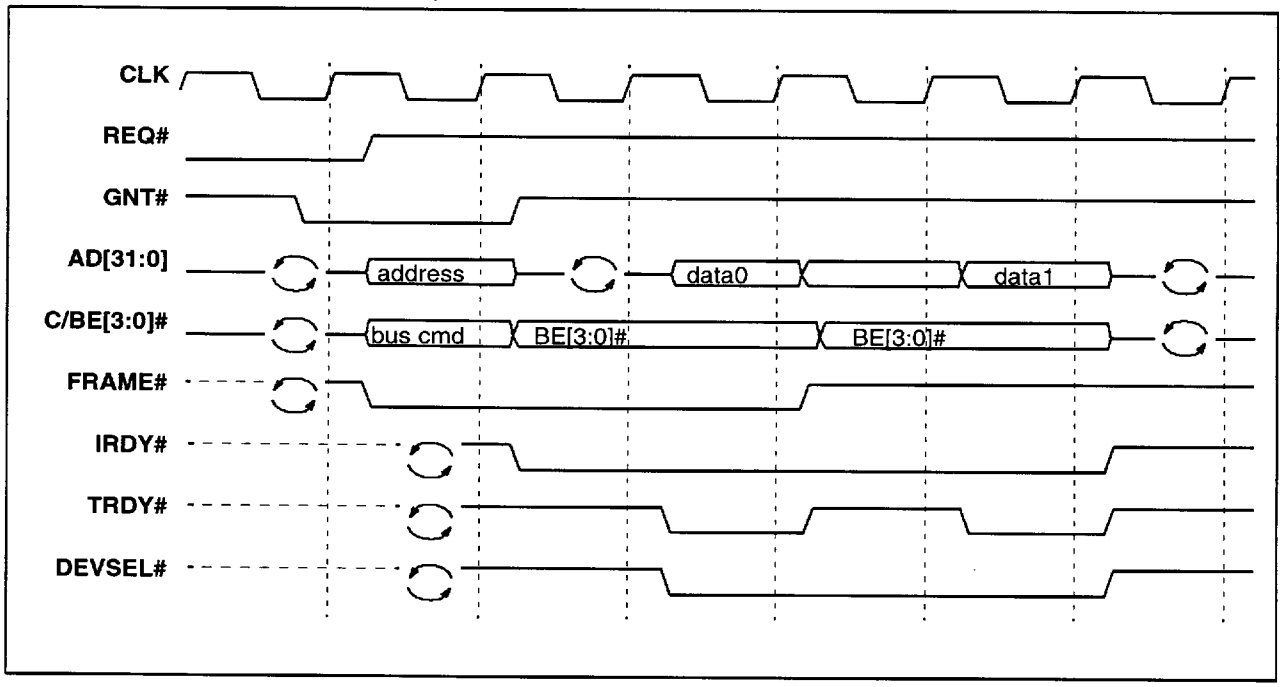


Figure 8. PCI Master read - multiple word



Note: The STG2000 does not generate fast back to back cycles as a bus master

Figure 9. PCI Target configuration cycle - Slave Configuration Write

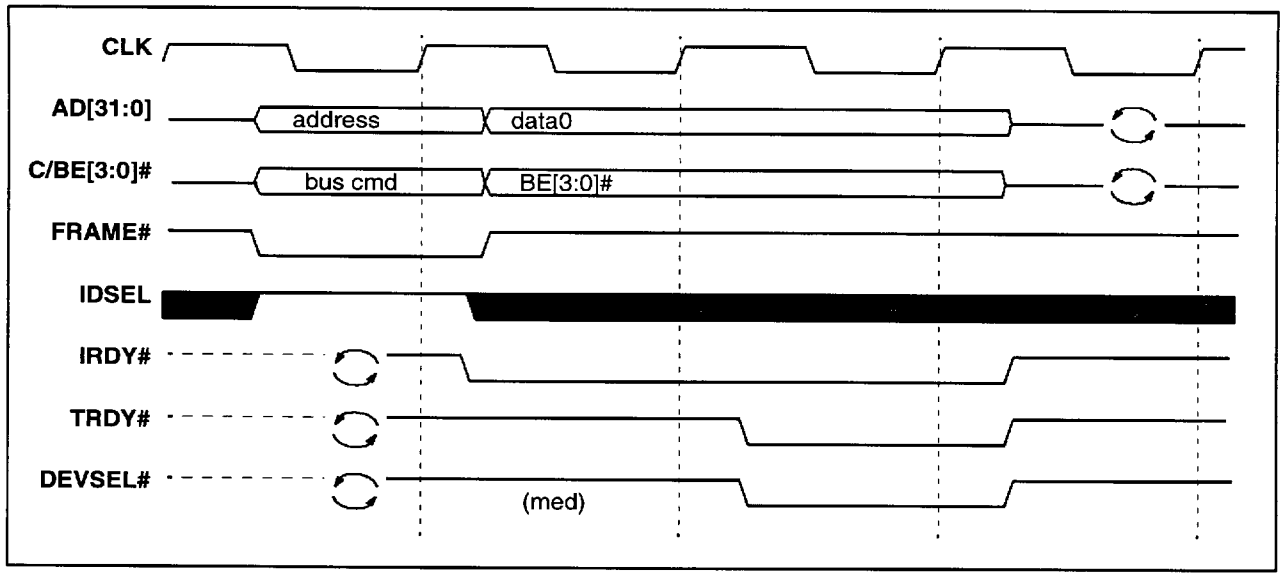


Figure 10. PCI Target configuration cycle - Slave Configuration Read

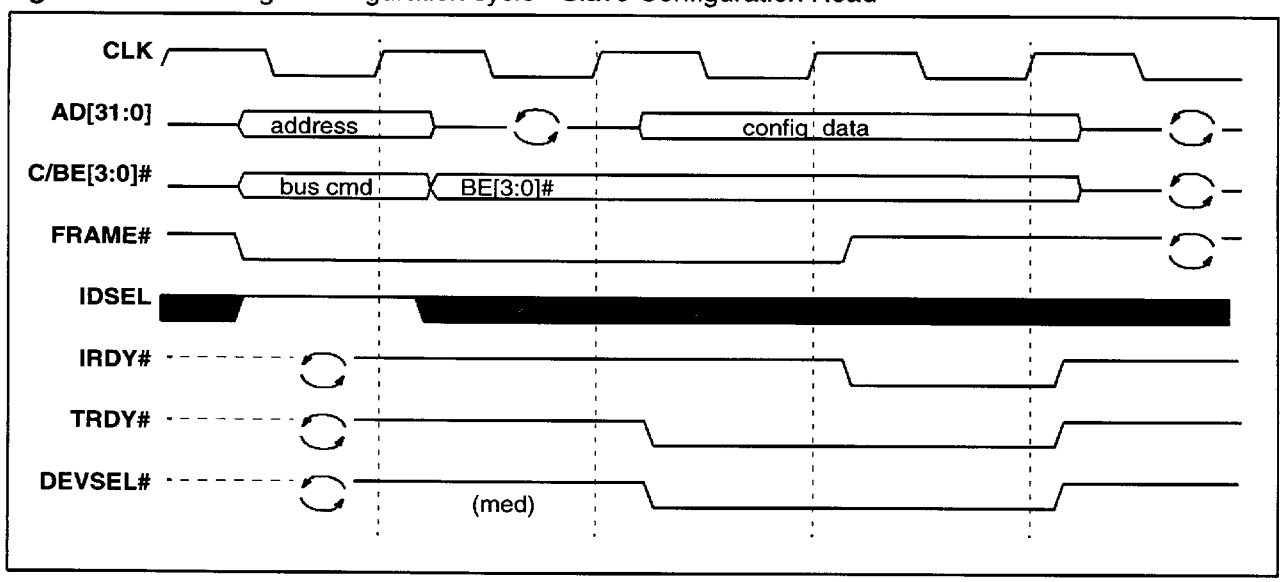


Figure 11. PCI basic arbitration cycle

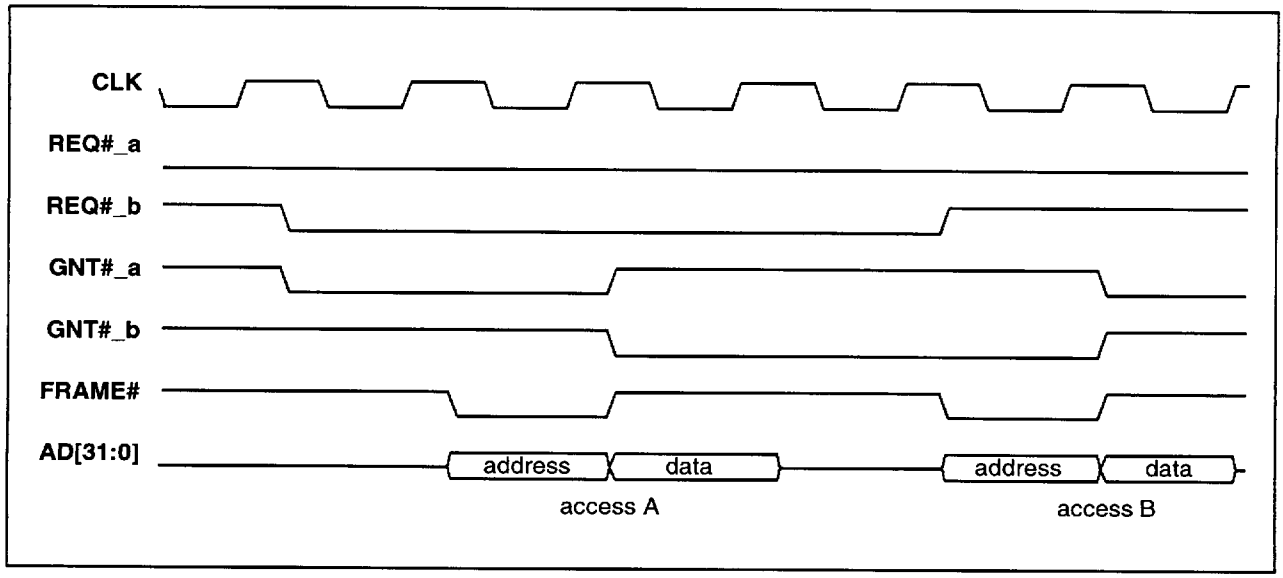
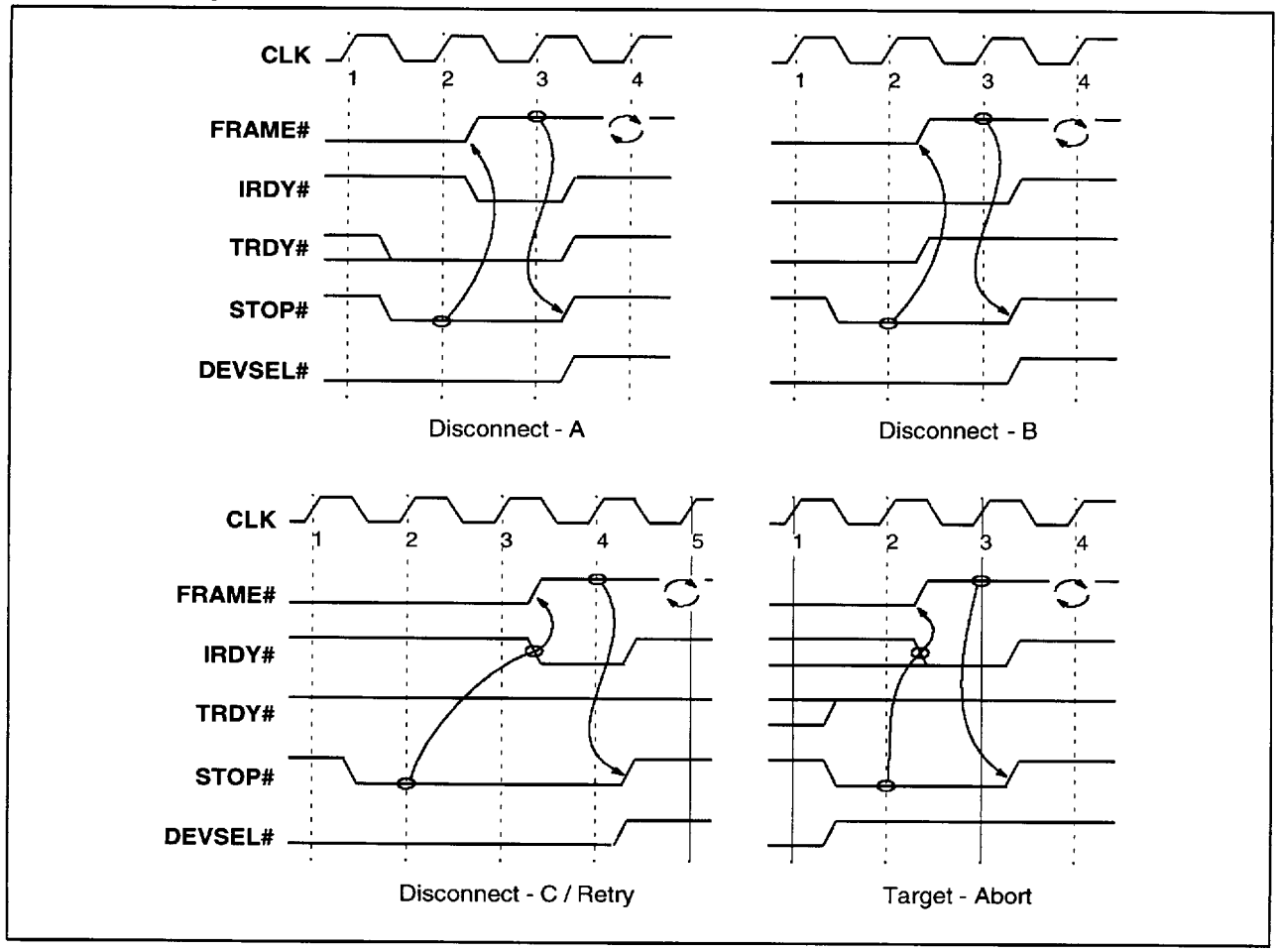


Figure 12. Target initiated termination



5 MEMORY AND PALETTE-DAC INTERFACE

5.1 DRAM MEMORY INTERFACE

The STG2000 DRAM memory interface is designed primarily for 4Mbit, symmetric address 256K×16, dual CAS# memory devices. The following DRAM memory cycles are supported by the STG2000:

- Random read (non-page mode access)
- Random read with extended data output
- Random write (non-page mode access)
- Fast page-mode read
- Hyper page-mode read with extended data output
- Page-mode write (late write)
- Page-mode write with non-persistent write-per-bit mask
- CAS-before-RAS refresh

The STG2000 can access pixels as 8-bit, 16-bit or 32-bit wide values. The DRAM allocated to the frame buffer is therefore configured to be addressed uniformly in either 8-bit, 16-bit or 32-bit quantities.

The STG2000 memory controller internally generates its own refresh timer. It will request a refresh cycle every 776 MCLK periods. At 50MHz, this represents a refresh request rate of 15.52µs. The refresh operation is exclusively performed by CAS-before-RAS DRAM refresh cycles.

DRAM memory configurations

The STG2000 memory is organized in banks. A memory system consists of one, two, or four banks of DRAM. Each bank consists of two 256K×16 DRAMs comprising 1MByte of storage organized as 256K×32. The STG2000 memory interface comprises a 32-bit DRAM data bus, two 9-bit DRAM address buses and the control signals required to manage up to 4 banks of memory with a 2-to-1 interleave. Figure 13 shows memory interface options for 1, 2 and 4MBytes of DRAM.

The STG2000 supports hyper page mode (extended data output) cycles in some configurations. They include 1MByte with either the STG 1732 or STG1764 DAC, and both 2MByte and 4MByte with the STG1764. The advantage is that very high data transfer rates can occur when using the EDO DRAMs. Bursts from a 64-bit wide EDO memory into the STG1764 occur at up to 400MByte/s. Bursts from a 32-bit 1MByte EDO memory into the STG1732 occur at 200MByte/s.

Standard DRAM is interleaved for improved performance in a 32-bit (STG1732) 2MByte design. This provides a 200MByte/s data transfer rate. Standard 4MByte DRAM designs are also interleaved into the STG1764 at a data transfer rate of 200MByte/s. A 1MByte standard DRAM memory can achieve a 100MByte/s data transfer rate.

Figure 13. 1, 2 and 4MByte DRAM memory configuration options

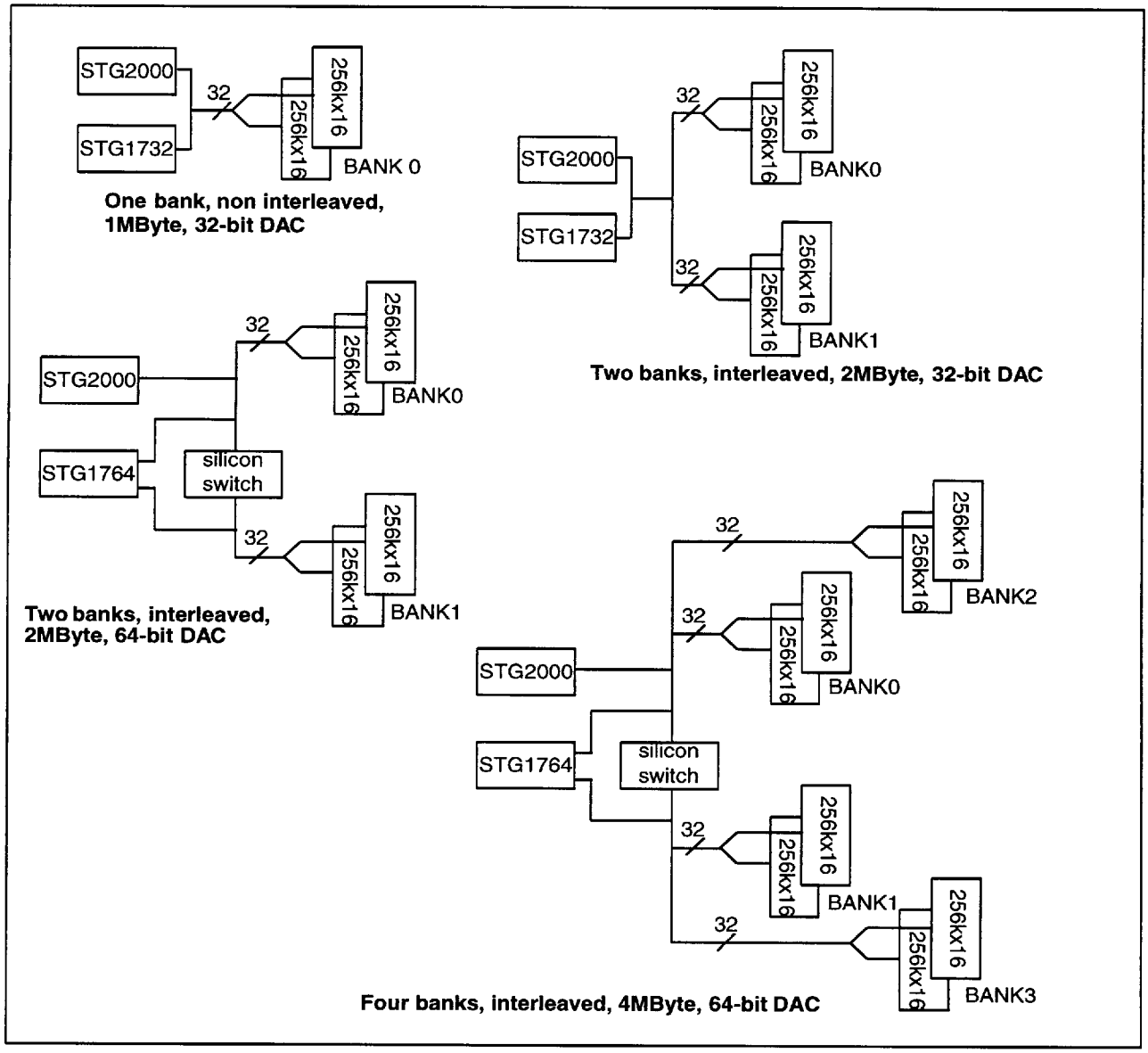


Figure 14. 1-2MByte DRAM configuration with the STG1732 Palette-DAC

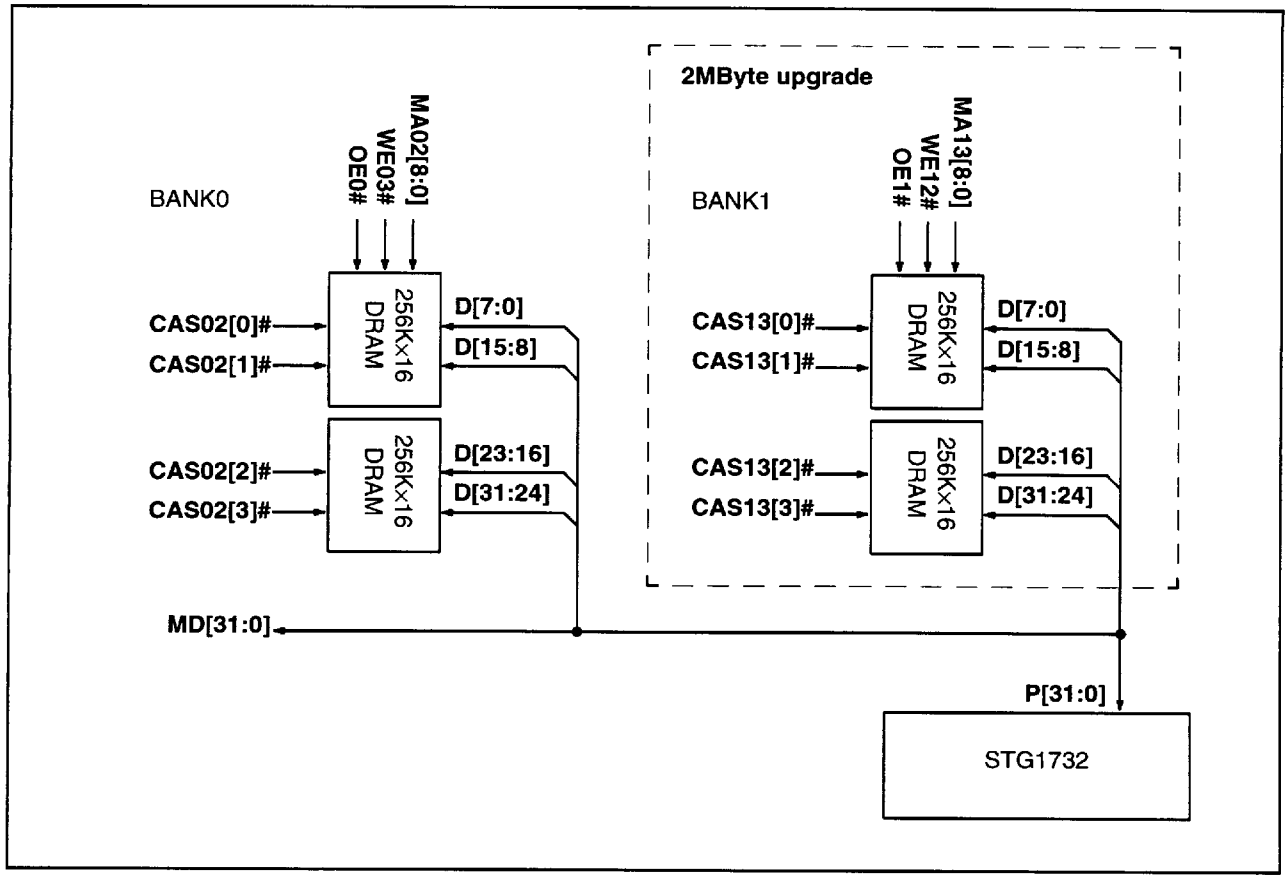
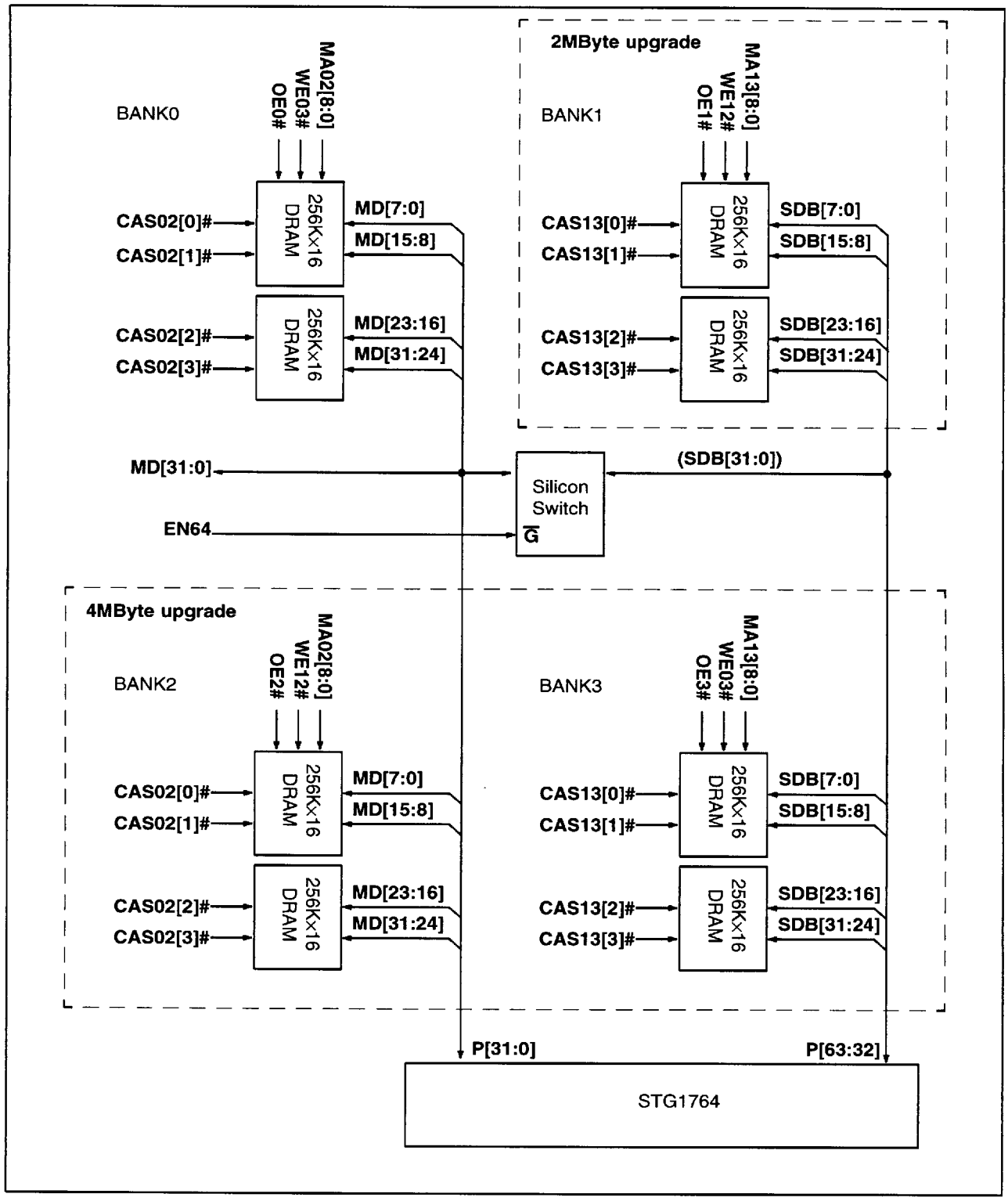


Figure 15. 1-4MByte DRAM configuration with the STG1764 Palette-DAC



DRAM interface timing specification

Figure 16. 4MByte DRAM read cycle timing diagram

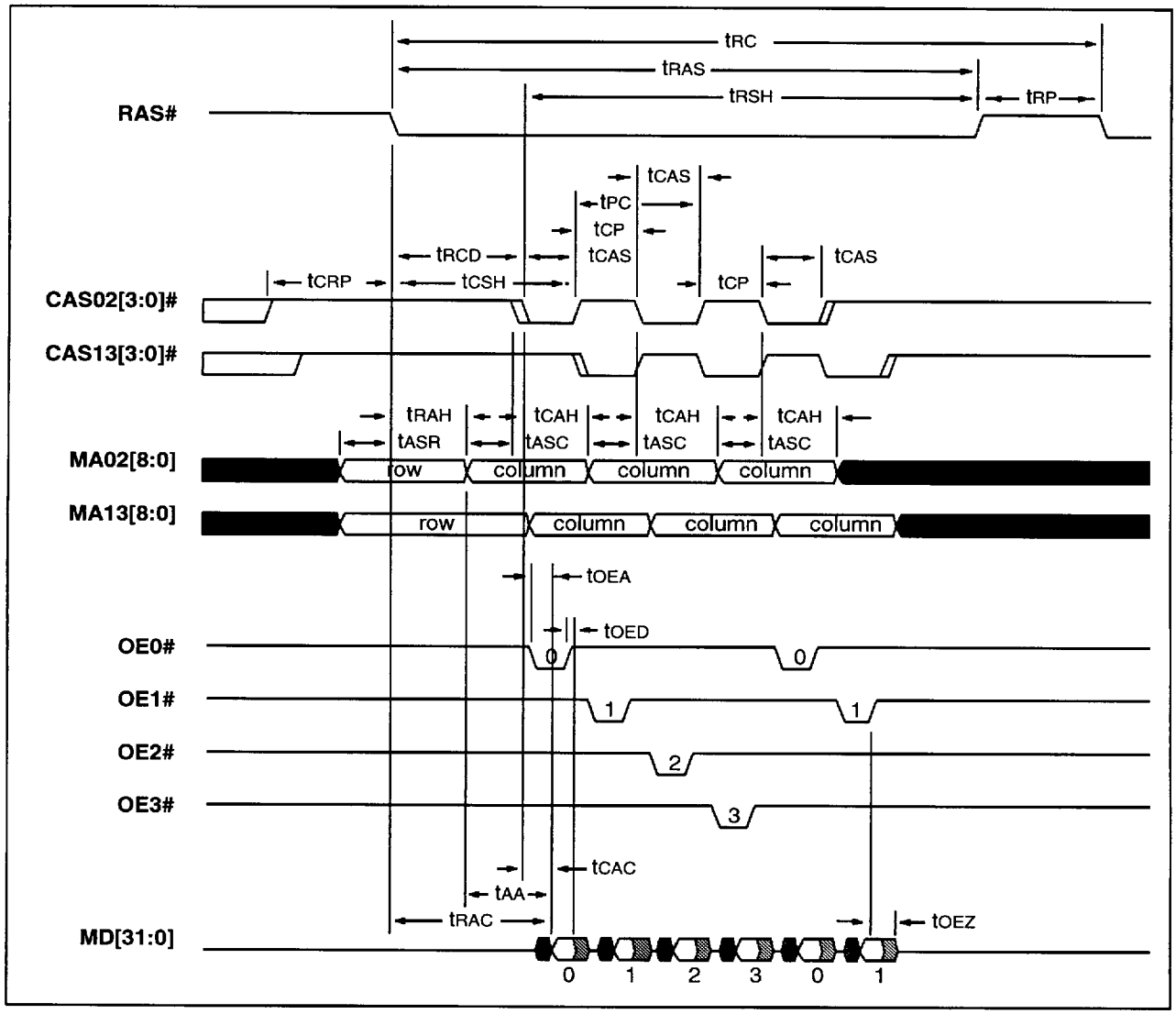


Table 3. 4MByte DRAM read cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tRC	Read cycle time	6TMCLK-5		ns	
tRAS	**RAS#** pulse width	3.5TMCLK-2		ns	
tRP	**RAS#** precharge time	2.5TMCLK-2		ns	
tCRP	**CASxx[3:0]#** to **RAS#** precharge time	3TMCLK-10		ns	
tCSH	**CASxx[3:0]#** hold time	3TMCLK-5		ns	
tRCD	**RAS#** to **CASxx[0:3]#** delay time	2TMCLK-5		ns	
tRSH	**RAS#** hold time	1.5TMCLK-2		ns	
tCP	**CASxx[3:0]#** precharge time (page mode)	TMCLK-5		ns	
tCAS	**CASxx[3:0]#** pulse width	TMCLK-2		ns	
tASR	Row address setup time	2		ns	
tASC	Column address setup time	2		ns	
tRAH	Row address hold time	TMCLK-5		ns	
tCAH	Column address hold time	TMCLK-5		ns	
tCAC	Access time from **CASxx[3:0]#**	TMCLK		ns	
tAA	Access time from column address	2TMCLK-5		ns	
tRAC	Access time from **RAS#**	3TMCLK-2		ns	
tPC	Fast page mode cycle time	2TMCLK-2		ns	
tOEA	Output enable time	TMCLK-7		ns	
tOED	Output disable to data invalid	0		ns	
tOEZ	**OEx#** rising to **MD[31:0]** high-z		7	ns	

NOTE

1 TMCLK is the period of the internal memory clock.

Figure 17. 1MByte DRAM hyper page mode read cycle timing diagram

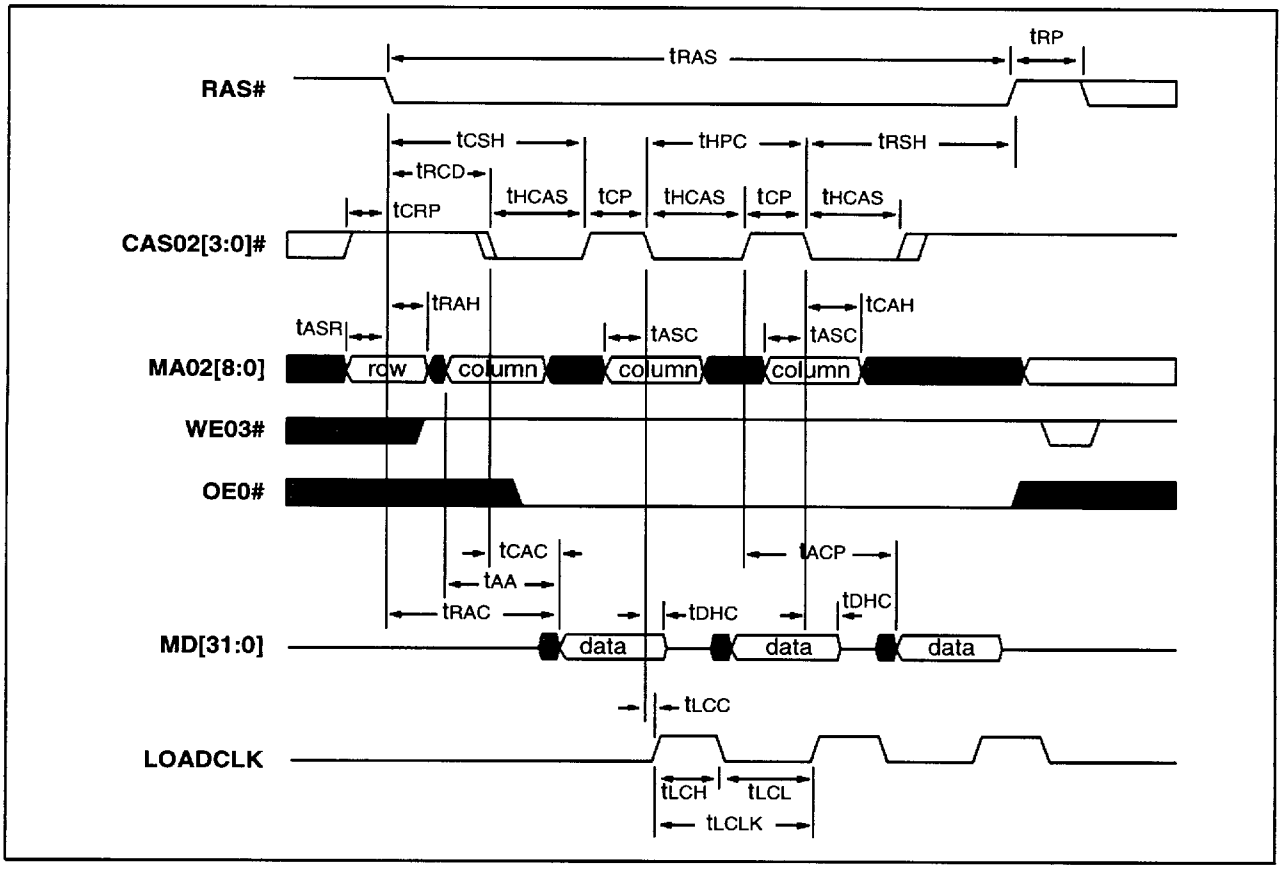


Table 4. 1, 2 and 4MByte DRAM hyper page mode read cycle timing parameters

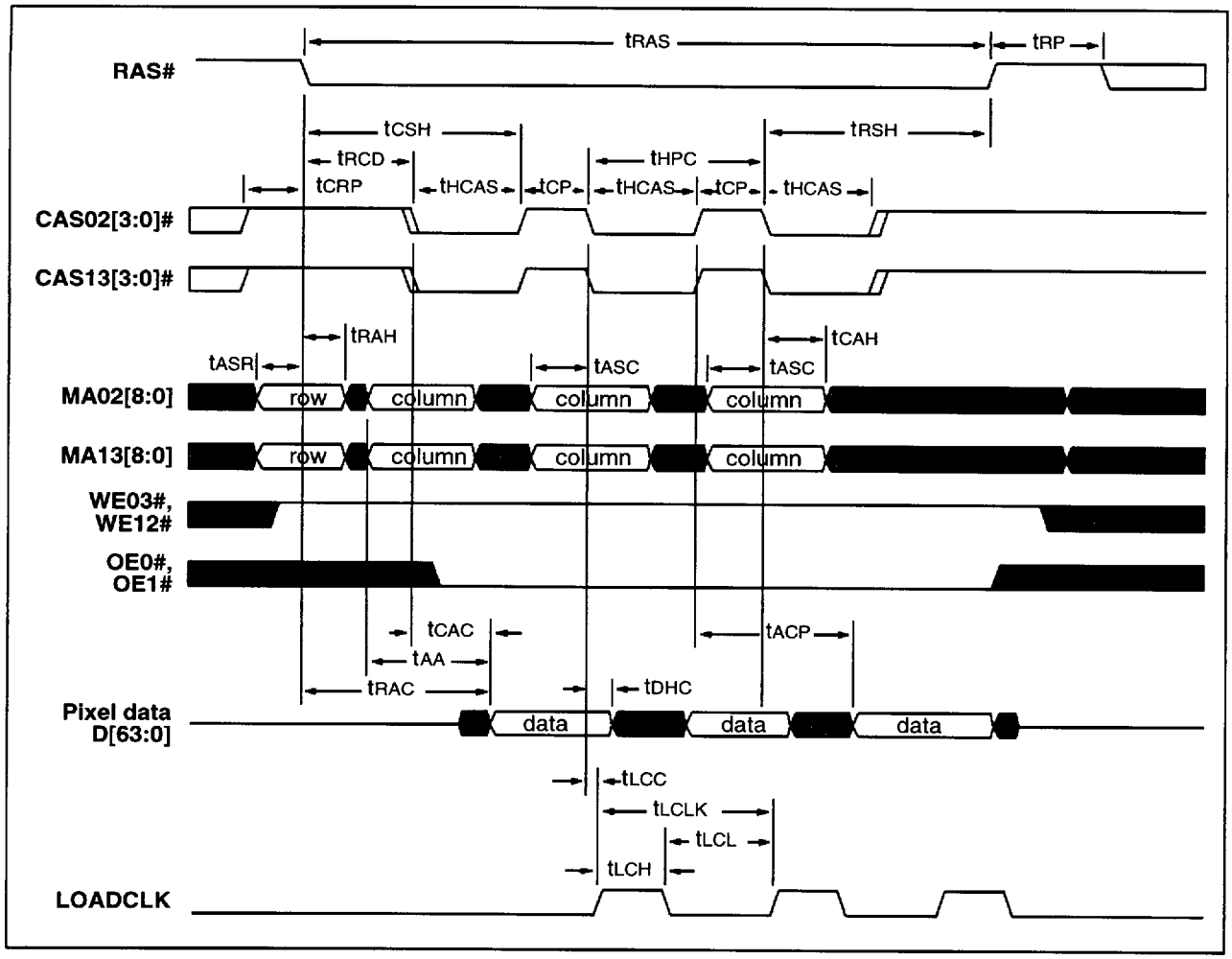
Symbol	Parameter	Min.	Max.	Unit	Notes
tRC	Read cycle time	6TMCLK-5		ns	
tRAS	**RAS#** pulse width	3.5TMCLK-2		ns	
tRP	**RAS#** precharge time	2.5TMCLK-2		ns	
tCRP	**CASxx[3:0]#** to **RAS#** precharge time	3TMCLK-10		ns	
tCSH	**CASxx[3:0]#** hold time	3TMCLK-5		ns	
tRCD	**RAS#** to **CASxx[0:3]#** delay time	2TMCLK-5		ns	
tRSH	**RAS#** hold time	TMCLK-2		ns	
tCP	**CASxx[3:0]#** precharge time (hyper page mode)	0.5TMCLK-2		ns	
tHCAS	**CASxx[3:0]#** pulse width (hyper page mode)	0.5TMCLK-2		ns	
tASR	Row address setup time	2		ns	
tASC	Column address setup time	2		ns	
tRAH	Row address hold time	TMCLK-5		ns	
tCAH	Column address hold time	TMCLK-5		ns	
tCAC	Access time from **CASxx[3:0]#**	TMCLK		ns	
tAA	Access time from column address	TMCLK-2		ns	

Symbol	Parameter	Min.	Max.	Unit	Notes
tRAC	Access time from **RAS#**	3TMCLK-2		ns	
tHPC	Hyper page mode read cycle time	TMCLK-2		ns	
tDHC	Data hold from **CASxx[3:0]#**	2		ns	
tACP	Access time from **CASxx[3:0]#** precharge	1.5TMCLK-5		ns	
tLCH	**LOADCLK** high pulse width	6		ns	
tLCL	**LOADCLK** low pulse width	6		ns	
tLCK	**LOADCLK** cycle time	18		ns	
tLCC	**LOADCLK** rising from **CASxx[3:0]#** active		0	ns	

NOTE

1 TMCLK is the period of the internal memory clock.

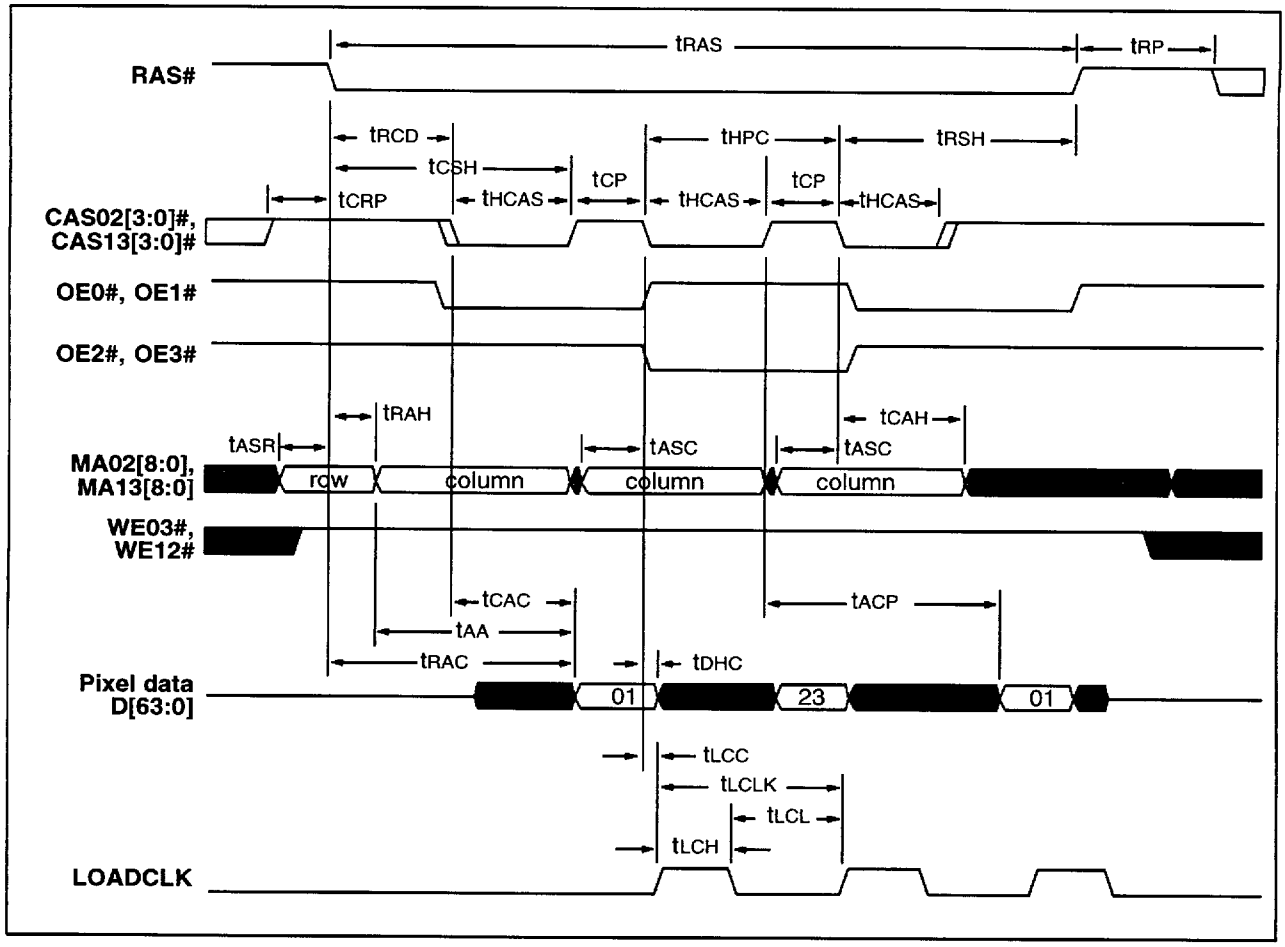
Figure 18. 2MByte DRAM hyper page mode read cycle timing diagram into STG1764



NOTE

1 The timing parameters for the 2MByte DRAM hyper page mode read cycle are given in Table 4.

Figure 19. 4MByte DRAM hyper page mode read cycle timing diagram into STG1764



NOTE

1 The timing parameters for the 4MByte DRAM hyper page mode read cycle are given in Table 4.

Figure 20. 4MByte DRAM write cycle timing diagram (**MA02[8:0]** and **MA13[8:0]** interleaved)

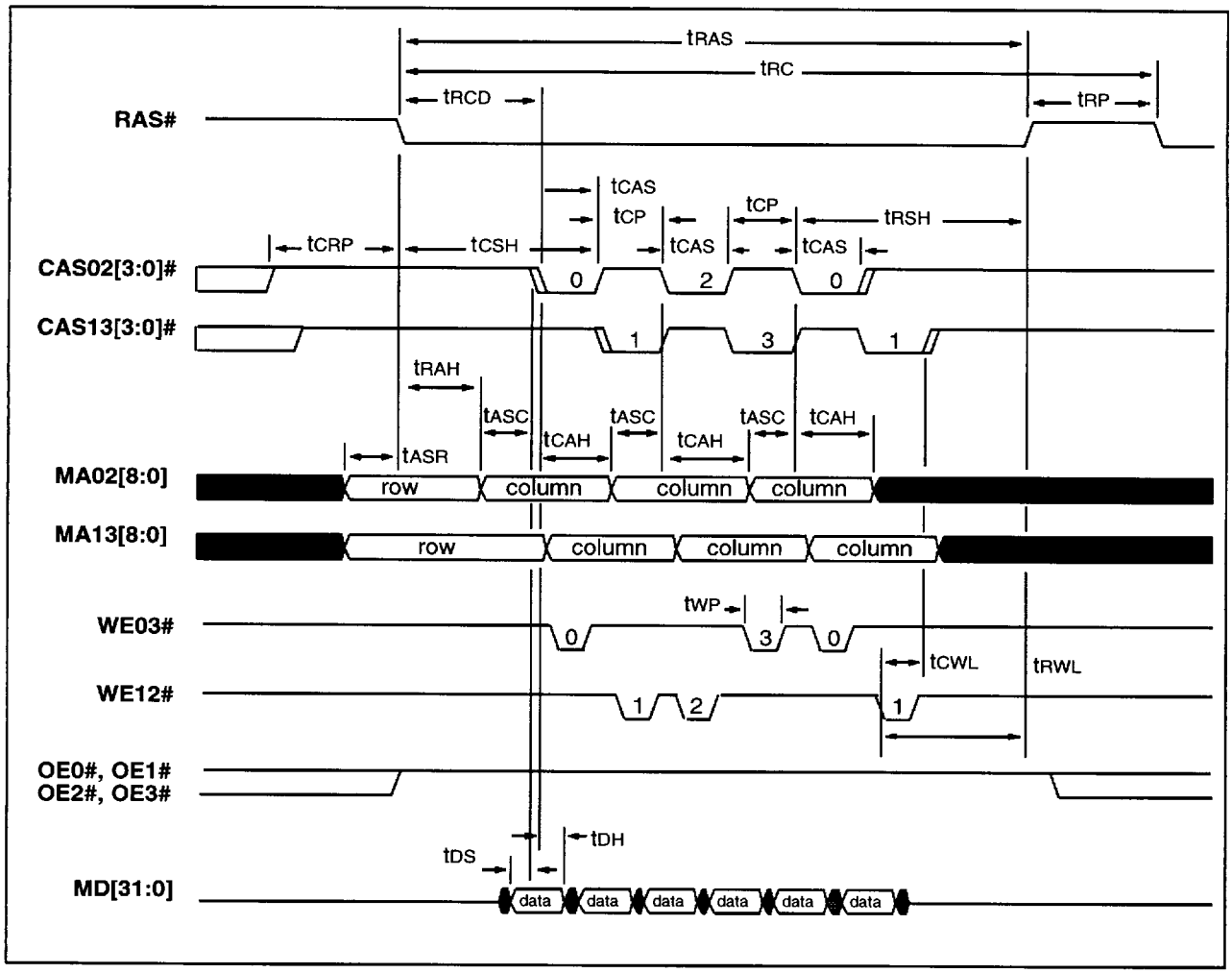


Table 5. 4MByte DRAM late write cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tRC	**Write cycle time**	6TMCLK-5		ns	
tRAS	**RAS#** pulse width	3.5TMCLK-2		ns	
tRP	**RAS#** precharge time	2.5TMCLK-2		ns	
tCRP	**CASxx[3:0]#** to **RAS#** precharge time	3TMCLK-10		ns	
tCSH	**CASxx[3:0]#** hold time	3TMCLK-5		ns	
tRCD	**RAS#** to **CASxx[0:3]#** delay time	2TMCLK-5		ns	
tRSH	**RAS#** hold time	1.5TMCLK-2		ns	
tCP	**CASxx[3:0]#** precharge time (page mode)	TMCLK-5		ns	
tCAS	**CASxx[3:0]#** pulse width (page mode)	TMCLK-2		ns	
tASR	Row address setup time	2		ns	
tASC	Column address setup time	2		ns	
tRAH	Row address hold time	TMCLK-5		ns	

Symbol	Parameter	Min.	Max.	Unit	Notes
tCAH	Column address hold time	TMCLK-5		ns	
tPC	Fast page mode cycle time	2TMCLK-2		ns	
tWP	Write command pulse width	0.5TMCLK		ns	
tCWL	Write command active to **CASxx[3:0]#** inactive	0.5TMCLK+2		ns	
tRWL	Write command active to **RAS#** inactive	0.5TMCLK+2			
tDS	Write data setup time	0.5TMCLK-2		ns	
tDH	Write data hold time	0.5TMCLK+2		ns	

NOTE

1 TMCLK is the period of the internal memory clock.

Figure 21. DRAM CAS# before RAS# refresh cycle timing diagram

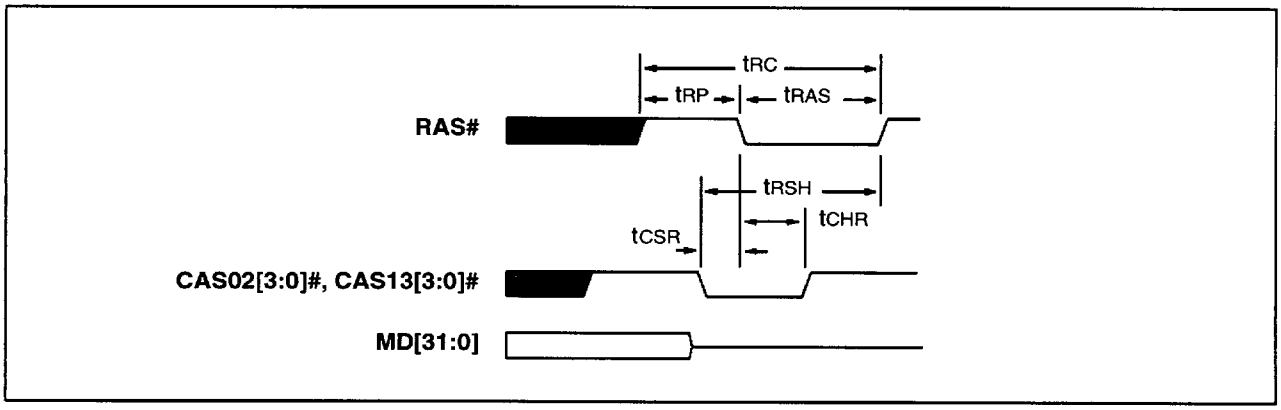


Table 6. DRAM CAS# before RAS# refresh cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tRC	**CAS# before RAS# cycle time**	6TMCLK-5		ns	
tRAS	**RAS#** pulse width	3.5TMCLK-2		ns	
tRP	**RAS#** precharge time	2.5TMCLK-2		ns	
tRSH	**RAS# hold time**	4TMCLK-5		ns	
tCSR	**CASxx[3:0]# setup time**	TMCLK-5		ns	
tCHR	**CASxx[3:0]# hold time**	TMCLK-5		ns	

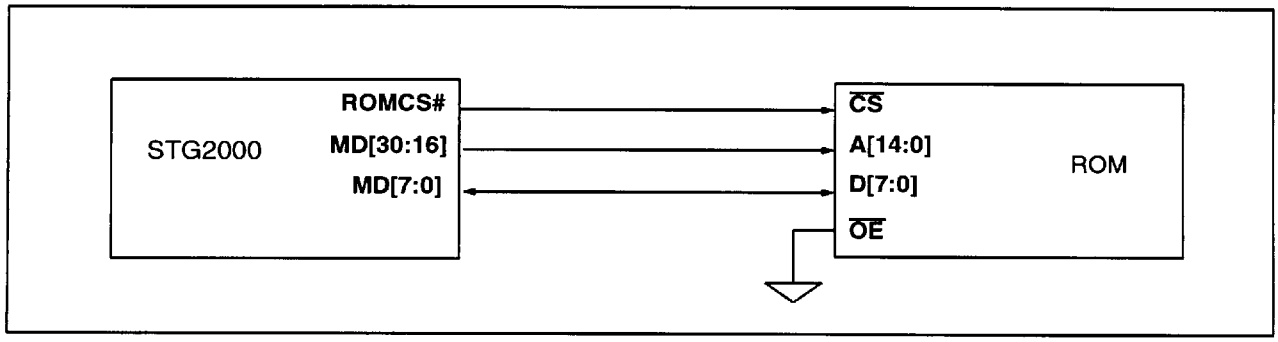
NOTE

1 TMCLK is the period of the internal memory clock.

5.2 ROM INTERFACE

BIOS and initialization code for the STG2000 is accessed from a 32KByte ROM.OTP or EPROM ROM may be selected The STG2000 memory bus interface signals **MDB[30:16]** and **MDB[7:0]** are used to address and read one of the 32KBytes of data respectively. The unique decode to the ROM device is provided by the **ROMCS#** chip select signal.

Figure 22. ROM interface



ROM interface timing specification

Figure 23. ROM interface timing diagram

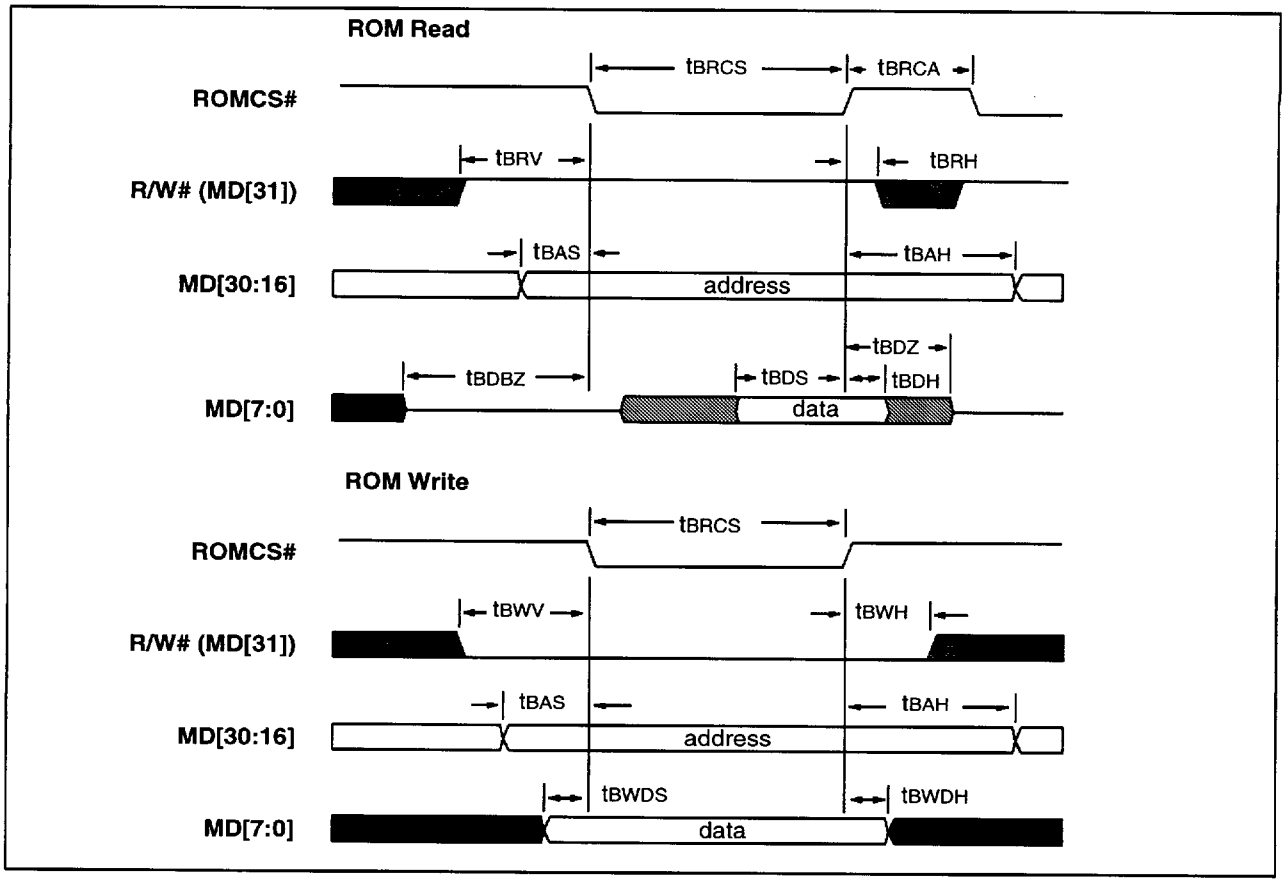


Table 7. ROM interface timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tBRCS	**ROMCS#** active pulse width	13TMCLK-5		ns	
tBRCA	**ROMCS#** precharge time	TMCLK-5		ns	
tBRV	Read valid to **ROMCS#** active	TMCLK-5		ns	
tBRH	Read hold from **ROMCS#** inactive	0.5TMCLK-5		ns	
tBAS	Address setup to **ROMCS#** active	TMCLK-5		ns	
tBAH	Address hold from **ROMCS#** inactive	0.5TMCLK-5		ns	
tBDBZ	Data bus high-z to **ROMCS#** active	TMCLK-5		ns	
tBDS	Data setup to **ROMCS#** inactive	10		ns	
tBDH	Data hold from **ROMCS#** inactive	0		ns	
tBDZ	Data high-z from **ROMCS#** inactive		TMCLK-5	ns	
tBWV	**R/W#** valid setup to **ROMCS#** active	TMCLK-5		ns	
tBWH	**R/W#** hold from **ROMCS#** inactive	0.5TMCLK-5		ns	
tBWDH	Write data hold from **ROMCS#** inactive	0.5TMCLK-5		ns	
tBWDS	ROM write data setup to **ROMCS#** active	TMCLK-5		ns	

NOTE

1 TMCLK is the period of the internal memory clock.

5.3 EEPROM INTERFACE

The STG2000 interface to the EEPROM is implemented via an industry standard Microwire bus. This 3-signal protocol uses a chip enable (**EECS**) to select the EEPROM. Data transfer is accomplished via a bidirectional serial data line (**EESD**) and clock (**EESCLK**).

The EEPROM is structured in a 128x8-bit word organization, such as the ST93C46A. This common format is available in a small outline (SO8) package which can easily be located in close proximity to the STG2000. The serial data transfer rate is low (<1MHz), hence signal routing is not critical. Details of the standard data format structure and software interface protocol for accessing the 1Kbit data are given in the SGS-THOMSON Datasheet for the ST93C46A [7]. Preprogrammed EEPROM devices for the STG2000 Multimedia Accelerator chipset are available from SGS-THOMSON with the part number NVCAATR.

The STG2000 automatically unlocks the EEPROM prior to sending a WRITE command. Following the write command it waits for the data line to be driven high, indicating completion of the write by the EEPROM. It then ends the user write request by sending an EWDS sequence to lock the EEPROM.

Figure 24. EEPROM power-on read sequence timing diagram

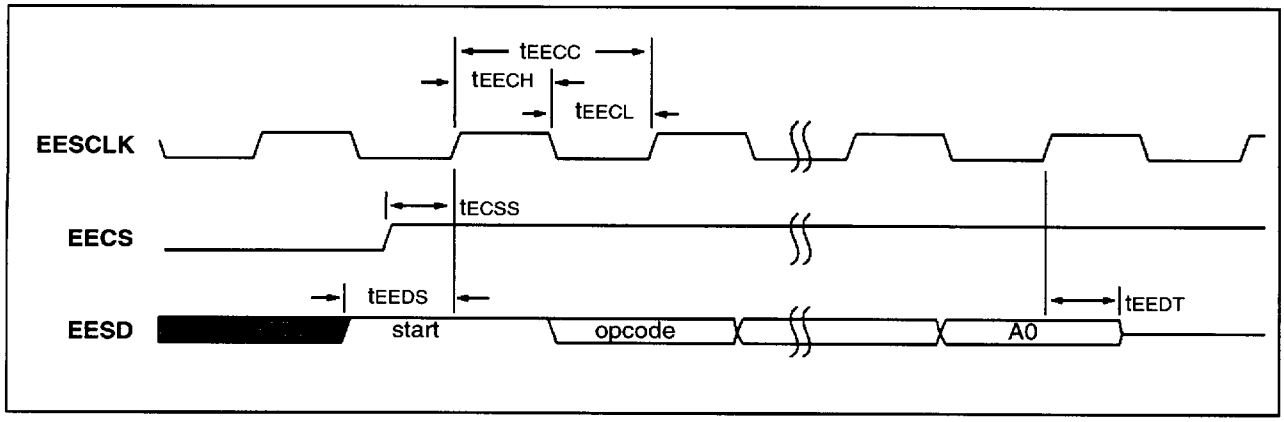


Table 8. EEPROM power-on read sequence timing parameters

Symbol	Parameter	Min.	Max.	Units	Notes
tEECC	**EESCLK** period	50		TMCLK	
tEECH	**EESCLK** high time	24		TMCLK	
tEECL	**EESCLK** low time	24		TMCLK	
tECSS	**EECS** high to **EESCLK** high	15		TMCLK	
tEEDS	**EESD** valid to **EESCLK** high	15		TMCLK	
tEEDT	**EESCLK** high to **EESD** inactive	15		TMCLK	

NOTE

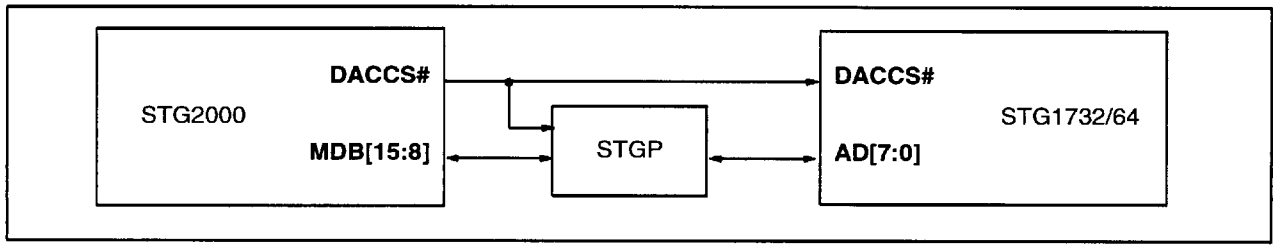
1 TMCLK is the period of the internal memory clock.

5.4 PALETTE-DAC INTERFACE

The STG1764 or STG1732 Palette-DAC interface comprises an 8-bit multiplexed address/data bus connecting to **MDB[15:8]** of the STG2000 memory bus. The unique decode to the Palette-DAC is provided by the **DACCS#** chip select signal. Each access is split into two phases; address and data.

In the address phase the falling edge of **DACCS#** latches the 4-bit address into the Palette-DAC and latches **MDB[15]** (Palette-DAC signal **AD[7]**) to identify whether the current access is a read or write.

Figure 25. DAC interface



Palette-DAC interface timing specification

Figure 26. **BLANK#** timing diagram

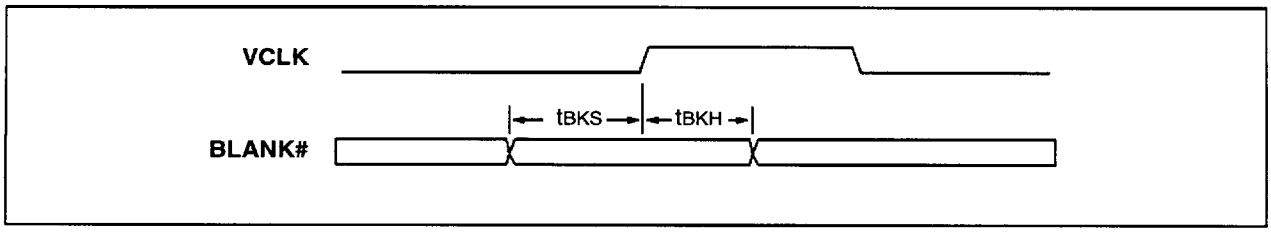


Table 9. **BLANK#** timing parameters

Symbol	Parameter	Min.	Max.	Units	Notes
tBKS	**BLANK#** set-up time	4.0		ns	
tBKH	**BLANK#** hold time	4.0		ns	

Figure 27. Palette-DAC interface read/write cycle timing diagram

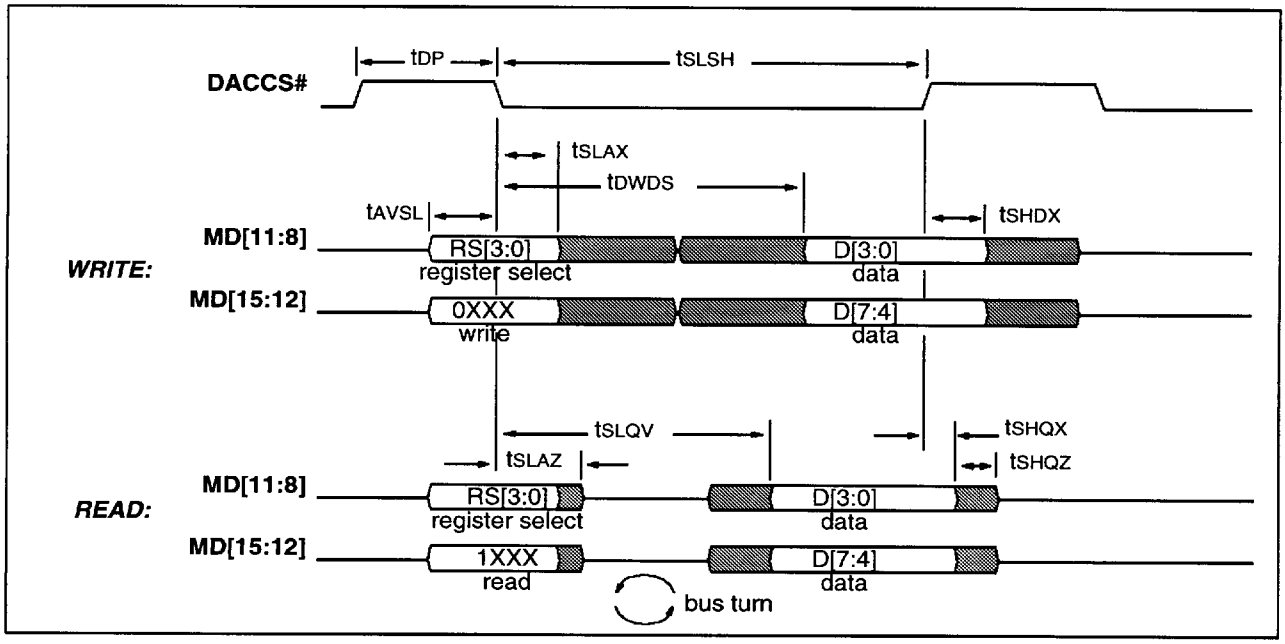


Table 10. Palette-DAC interface read/write cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tDP	DAC interface precharge time	3TMCLK-5		ns	DAC write cycle
tSLSH	**DACCS#** pulse time	3TMCLK-5		ns	DAC read cycle
tAVSL	Address setup time	1.5TMCLK-5		ns	Game Port read/write cycle
tSLAX	Address hold time	0		ns	All accesses
tDWDS	Write data setup time		0.5TMCLK+10	ns	Write cycle
tSHDX	Write data hold time	0.5TMCLK-10		ns	Write cycle
tSLAZ	Address high-z time		10	ns	Read cycle
tSLQV	Read access time from **DACCS#** active	2TMCLK-10		ns	Read cycle
tSHQX	Read data hold time from **DACCS#** inactive	0		ns	Read cycle
tSHQZ	Output turn-off delay		TMCLK-5	ns	Read cycle

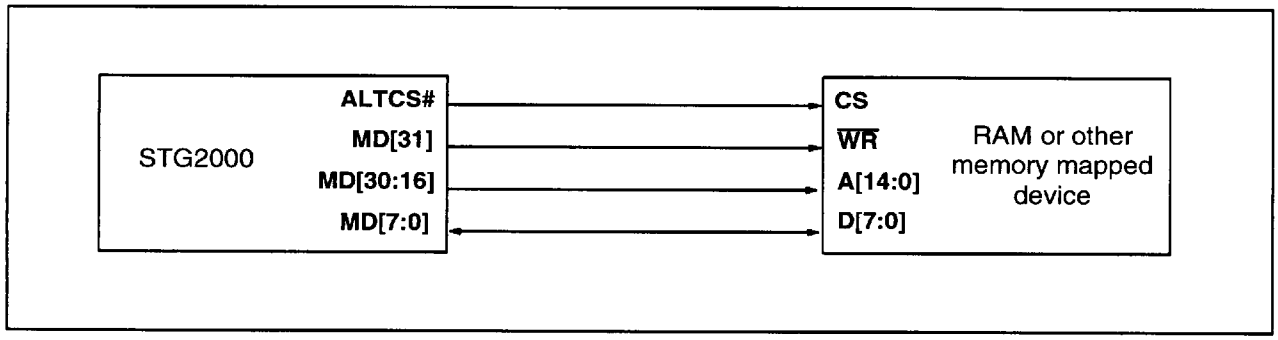
NOTE

1 TMCLK is the period of the internal memory clock.

5.5 ALTCS# INTERFACE

The STG2000 can access 32KBytes of read/write memory. The STG2000 memory bus interface signals **MDB[30:16]** and **MDB[7:0]** are used to address and access one of the 32KBytes of data respectively. **MDB[31]** provides an indication of a read or write cycle. The unique decode to this 32KByte device is provided by the **ALTCS#** chip select signal.

Figure 28. ROM interfaces



ALTCS# interface timing specification

Figure 29. ALTCS# interface timing diagram

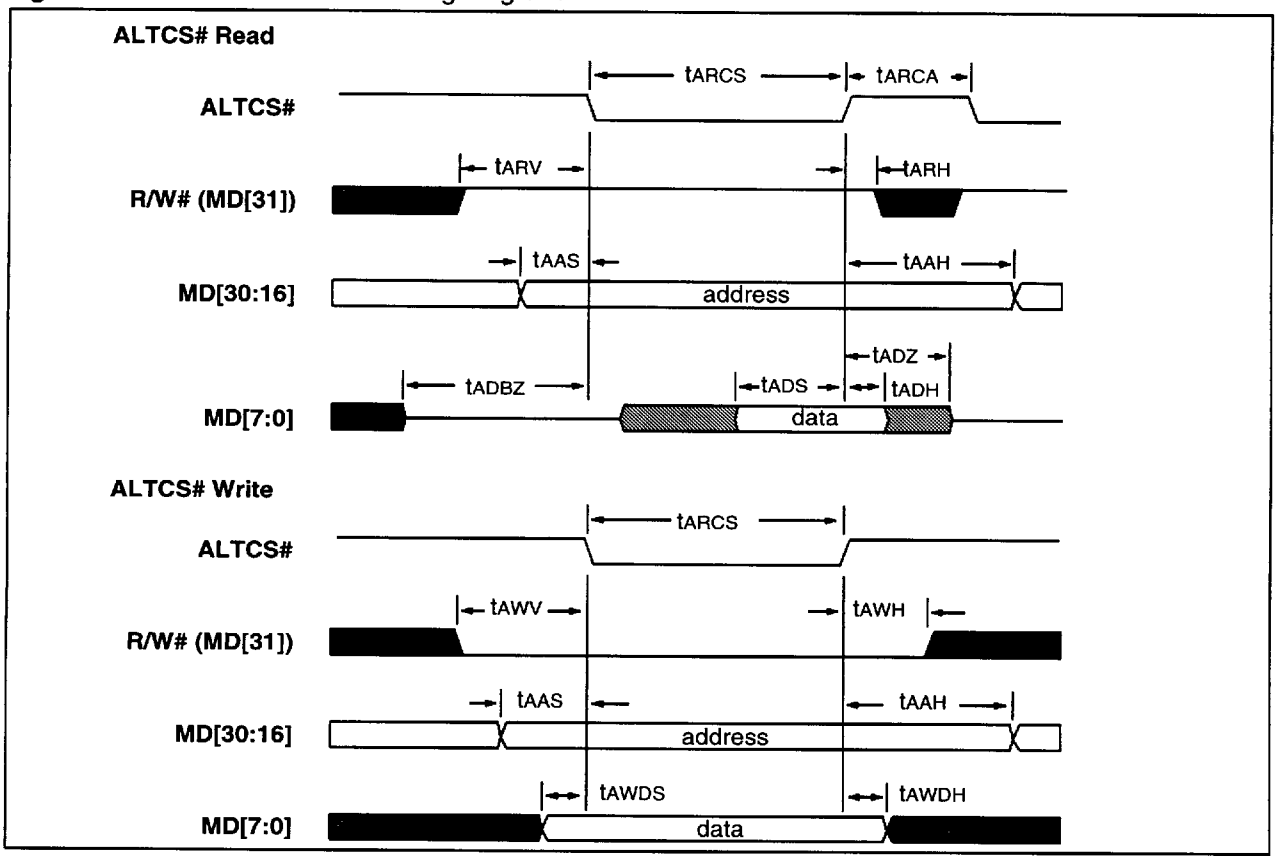


Table 11. ALTCS# interface timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tARCS	**ALTCS#** pulse width	13TMCLK-7		ns	
tARCA	**ALTCS#** precharge time	TMCLK-5		ns	
tARV	Read valid to **ALTCS#** active	TMCLK-5		ns	
tARH	Read hold from **ALTCS#** inactive	0.5TMCLK-5		ns	
tAAS	Address setup to **ALTCS#** active	TMCLK-5		ns	
tAAH	Address hold from **ALTCS#** inactive	0.5TMCLK-5		ns	
tADBZ	Data bus high-z to **ALTCS#** active	TMCLK-5		ns	
tADS	Data setup to **ALTCS#** inactive	10		ns	
tADH	Data hold from **ALTCS#** inactive	0		ns	
tADZ	Data high-z from **ALTCS#** inactive		TMCLK-5	ns	
tAWV	**R/W#** valid setup to **ALTCS#** active	TMCLK-5		ns	
tAWH	**R/W#** hold from **ALTCS#** inactive	0.5TMCLK-5		ns	
tAWDH	Write data hold from **ALTCS#** inactive	0.5TMCLK-5		ns	
tAWDS	Write data setup **ALTCS#** active	TMCLK-5		ns	

NOTE

1 TMCLK is the period of the internal memory clock.

6 AUDIO CODEC INTERFACE

The audio codec interface supports the Analog Devices AD1848 or equivalent. This is a mixed signal device that provides 16-bit stereo, multiple source audio capture and playback capability. The STG2000 audio codec interface, shown in Figure 30, does not use the interrupt or DMA features of the codec. The interface comprises an 8-bit data bus, two address bits and independent read and write strobes. The codec may be placed in a power-saving mode by asserting **AUPD#**.

The interface for designs using the NVASGP ASIC and I^2S DAC is shown in Figure 31.

Figure 30. Audio codec interface

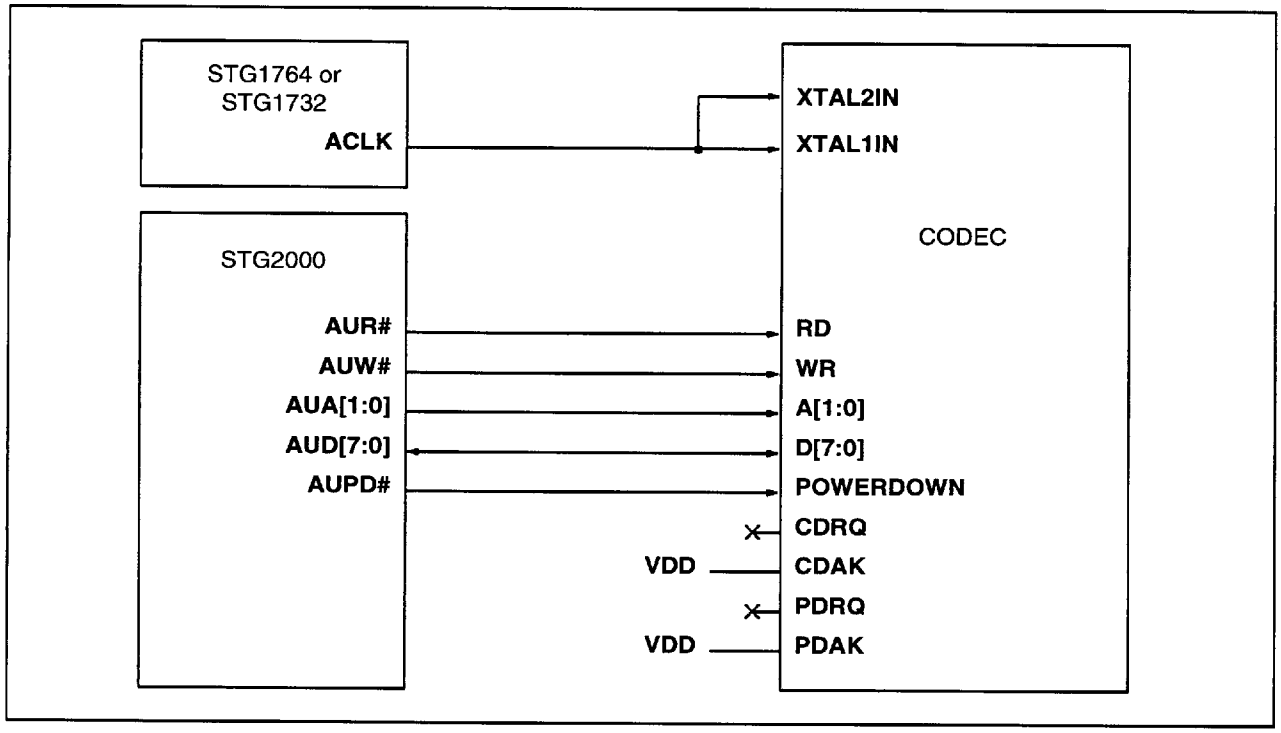
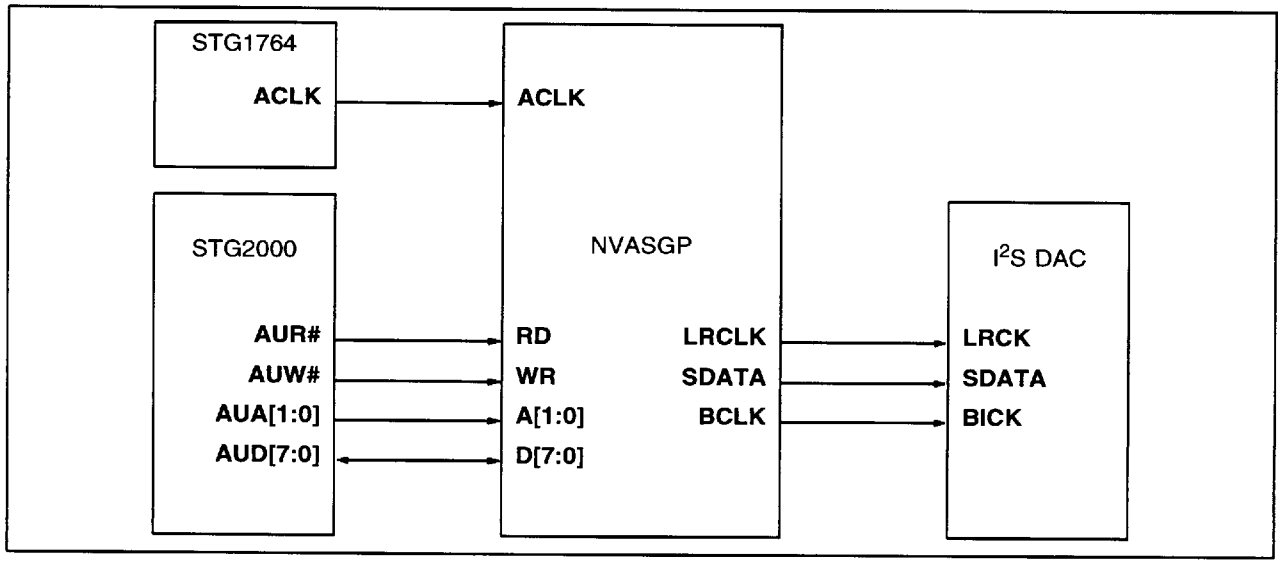


Figure 31. Serial DAC interface



6.1 AUDIO CODEC INTERFACE TIMING SPECIFICATION

Figure 32. Audio codec interface write cycle timing diagram

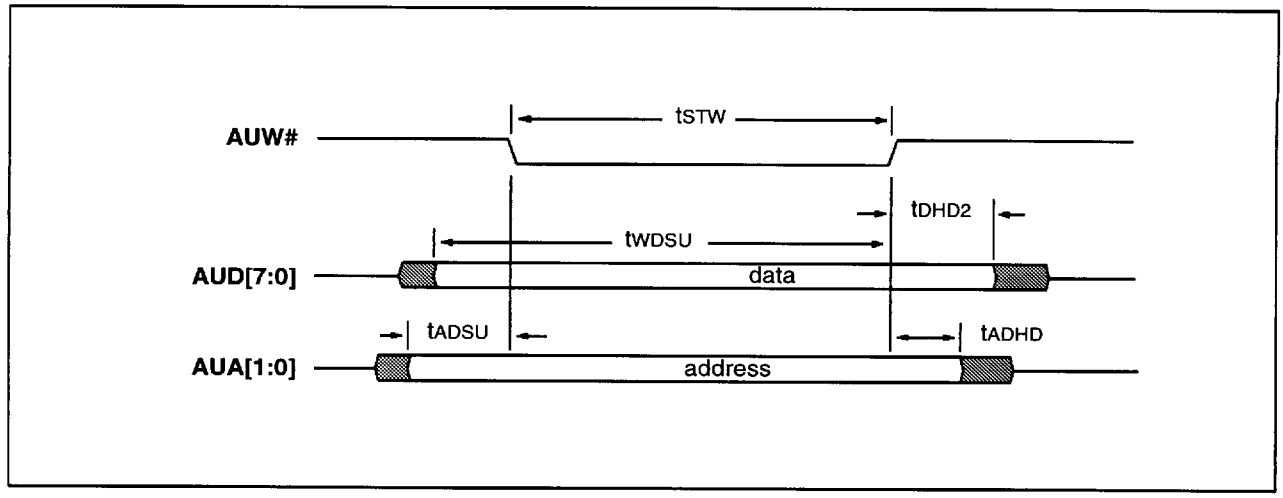


Table 12. Audio codec interface write cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tSTW	**AUW#** strobe width	13TMCLK-10		ns	1
tWDSU	**AUD[7:0]** setup to **AUW#** rising	17TMCLK-20		ns	1
tADSU	**AUA[1:0]** setup to **AUW#** falling	4TMCLK-20		ns	1
tADHD	**AUA[1:0]** hold from **AUW#** rising	3TMCLK-20	t.b.d.	ns	1
tDHD2	**AUD[7:0]** hold from **AUW#** rising	7TMCLK-20	t.b.d.	ns	1

NOTE

1 TMCLK = period of the internal memory clock

Figure 33. Audio codec interface read cycle timing diagram

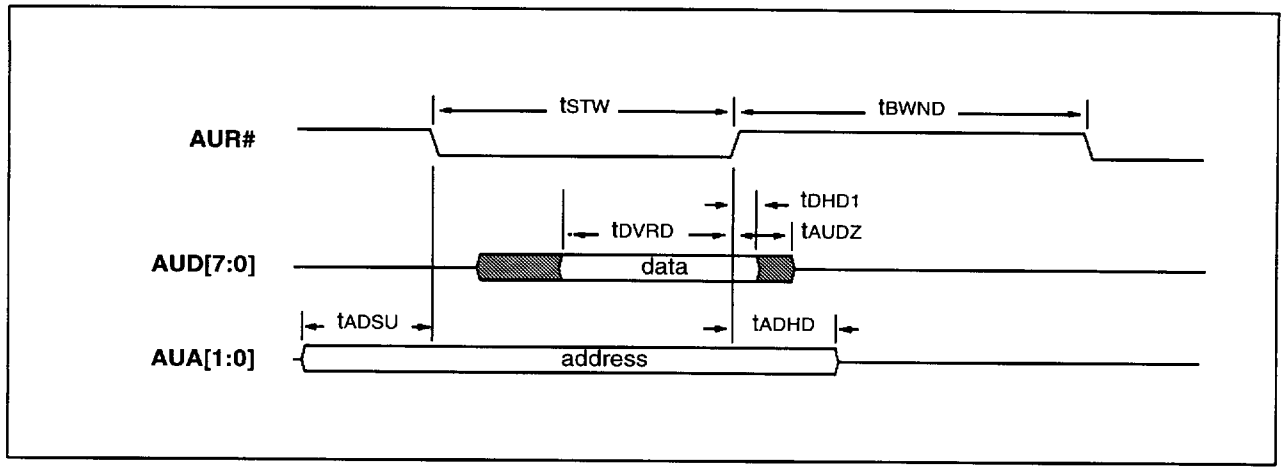


Table 13. Audio codec interface read cycle timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tSTW	**AUR#** strobe width	13TMCLK-10		ns	1
tBWND	**AUR#** rising to **AUR#** falling	15TMCLK-10		ns	1
tDVRD	**AUD[7:0]** valid to **AUR#** rising	20	t.b.d.	ns	
tADSU	**AUA[1:0]** setup to **AUR#** falling	4TMCLK-20		ns	1
tADHD	**AUA[1:0]** hold from **AUR#** rising	3TMCLK-20		ns	1
tDHD1	**AUD[7:0]** hold from **AUR#** rising	0		ns	
tAUDZ	**AUR#** rising to **AUD[7:0]** high-z		14TMCLK-20	ns	1

NOTE

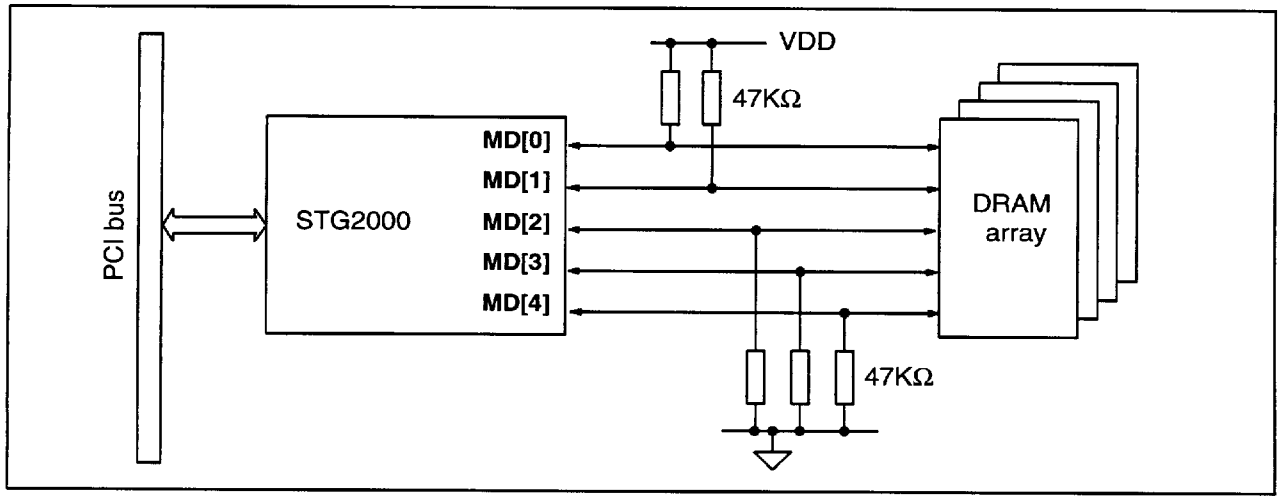
1 TMCLK = period of the internal memory clock

7 POWER-ON RESET CONFIGURATION

The STG2000 latches its configuration on the trailing edge of **RST#/RESET#** and holds its system bus interface in a high impedance state until this time. Normally the configuration is read from the BIOS which is located on the memory data bus. The memory interface drives **RAS#** and **OE#** inactive during this period.

In motherboard designs the BIOS will typically be merged with that of the system, hence the configuration information must be transferred in another manner. To accomplish this, pull-up or pull-down resistors are connected to the **MD[7:0]** bus as appropriate. In the STG2000 only bits [4:0] are significant. Since there are no internal pull-up or pull-down resistors and the data bus should be floating during reset, a resistor value of 47KΩ should be sufficient.

Figure 34. Planar implementation of STG2000 on the PCI bus



Power-on reset MD[7:0] bit assignments

7	6	5	4	3	2	1	0
Reserved			Bus Type	Board Type		Frame Buffer Type	

[7:5] Reserved

[4] Bus Type
0 = PCI bus
1 = VL-bus

[3:2] Board Type
00 = Motherboard
01 = Adapter #1 Note: Normally add-on cards will use the Adapter #1 configuration.
10 = Adapter #2
11 = Adapter #3

[1:0] Frame Buffer Type
00 = VRAM
01 = Illegal
10 = Illegal
11 = DRAM

8 ELECTRICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Min.	Max.	Units	Notes
VDD	DC supply voltage		3.6	V	
	Voltage on input and output pins	GND-1.0	7.5	V	
TS	Storage temperature (ambient)	-55	125	°C	
TA	Temperature under bias	0	85	°C	

NOTE

1 Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8.2 DC SPECIFICATIONS

Table 14. DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive supply voltage	3.0	3.3	3.6	V	
IIN	Input current (signal pins)			±10	µA	1, 2
PDmax	Power dissipation			1.7	W	

NOTES

1 Includes high impedance output leakage for all bi-directional buffers with tri-state outputs

2 VDD = max, GND ≤ VIN ≤ VDD

Table 15. Parameters applying to VL-bus interface pins

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CIN	Input capacitance		10	12	pF	
COUT	Output load capacitance		10	175	pF	
VIH	Input logic 1 voltage	2.0		5.5	V	
VIL	Input logic 0 voltage	-0.5		0.8	V	
VOH	Output logic 1 level	2.4			V	
VOL	Output logic 0 level			0.5	V	
IOL	Output load current, logic 0 level			8	mA	

Table 16. Parameters applying to PCI interface pins

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CIN	Input capacitance	5		10	pF	
COUT	Output load capacitance	5		50	pF	
Parameters for 5V signaling environment only:						
VIH	Input logic 1 voltage	2.0		5.75	V	
VIL	Input logic 0 voltage	-0.5		0.8	V	
VOH	Output logic 1 level	2.4			V	
VOL	Output logic 0 level			0.55	V	
IOH	Output load current, logic 1 level			-2	mA	
IOL	Output load current, logic 0 level			3 or 6	mA	1

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
Parameters for 3.3V signaling environment only:						
VIH	Input logic 1 voltage	0.475VDD		VDD+0.5	V	
VIL	Input logic 0 voltage	-0.5		0.325VDD	V	
VOH	Output logic 1 level	0.9VDD			V	
VOL	Output logic 0 level			0.1VDD	V	
IOH	Output load current, logic 1 level			-0.5	mA	
IOL	Output load current, logic 0 level			1.5	mA	

NOTE

1 3mA for all signals except **FRAME#**, **TRDY#**, **IRDY#**, **DEVSEL#**, **STOP#** and **SERR#** which have IOL of 6mA.

Table 17. Parameters applying to all signal pins except VL-bus and PCI interfaces

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CIN	Input capacitance		10	12	pF	
COUT	Output load capacitance		10	50	pF	
VIH	Input logic 1 voltage	2.0		5.75	V	
VIL	Input logic 0 voltage	-0.5		0.8	V	
VOH	Output logic 1 level	2.4			V	
VOL	Output logic 0 level			0.4	V	
IOH	Output load current, logic 1 level			-1	mA	
IOL	Output load current, logic 0 level			1	mA	

8.3 OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
TC	Ambient operating temperature	0	N/A	70	°C	

9 PACKAGE DIMENSION SPECIFICATION

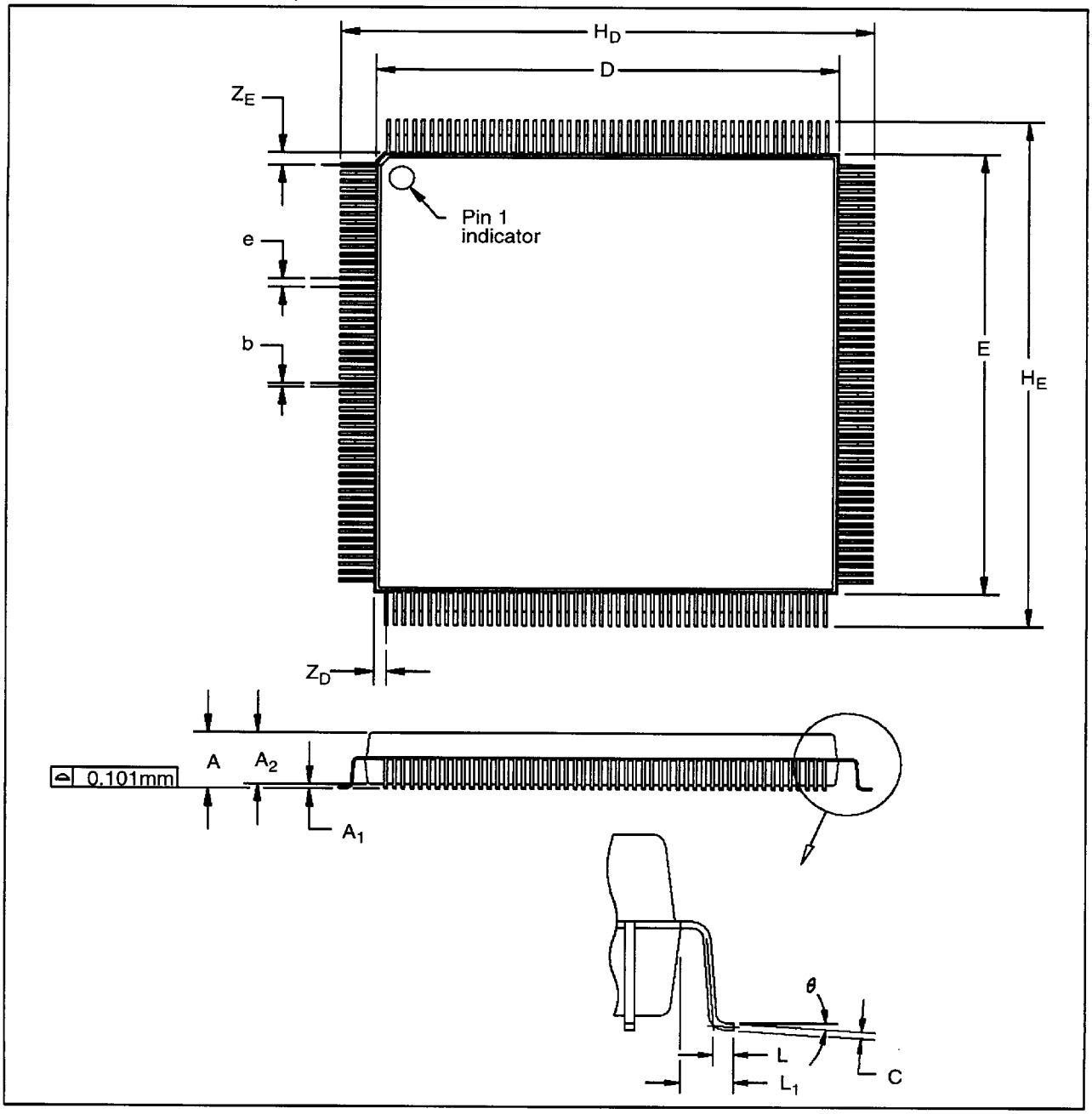
9.1 208 PIN PLASTIC QUAD FLAT PACK

Table 18. STG2000 208 pin Plastic Quad Flat Pack dimensions

REF (see Figure 35).	CONTROL DIMENSIONS - mm			ALTERNATIVE DIMENSIONS - inches			NOTES
	MIN	NOM	MAX	MIN	NOM	MAX	
A			4.07			0.160	
A1	0.25			0.010			
A2	3.24		3.74	0.128		0.147	
b	0.16		0.30	0.006		0.012	
C	0.12		0.20	0.005		0.008	
D	27.80		28.20	1.095		1.110	
E	27.80		28.20	1.095		1.110	
e		0.50			0.020		BSC
HD	30.35		30.85	1.195		1.215	
HE	30.35		30.85	1.195		1.215	

REF (see Figure 35).	CONTROL DIMENSIONS - mm			ALTERNATIVE DIMENSIONS - inches			NOTES
	MIN	NOM	MAX	MIN	NOM	MAX	
L	0.40		0.60	0.016		0.024	
L1		1.30			0.051		
ZD		1.25			0.049		
ZE		1.25			0.049		
θ	0		8	0		8	Degrees

Figure 35. STG2000 208 pin Plastic Quad Flat Pack dimension reference



10 REFERENCES

1 STG2000 *Multimedia Accelerator Datasheet*, SGS-THOMSON Microelectronics, April 1996, SGS-THOMSON Document Number: 42 1653 04 (this document)

2 STG1732/64 *Palette-DAC Datasheet*, SGS-THOMSON Microelectronics, June 1995, SGS-THOMSON Document Number: 42 1648 02

3 *STG2000 Reference Design Kit (RDK), Design Guide*, SGS-THOMSON Microelectronics, April 1996, SGS-THOMSON Document Number: 72 OEK 290 03

4 ST93C46A, ST93C46C, ST93C46T *Serial access CMOS 1K bit EEPROM Datasheet*, SGS-THOMSON Microelectronics, August 1994

11 ORDERING INFORMATION

Device	Package	Part number
STG2000	208 pin PQFP	STG2000XC

APPENDICES

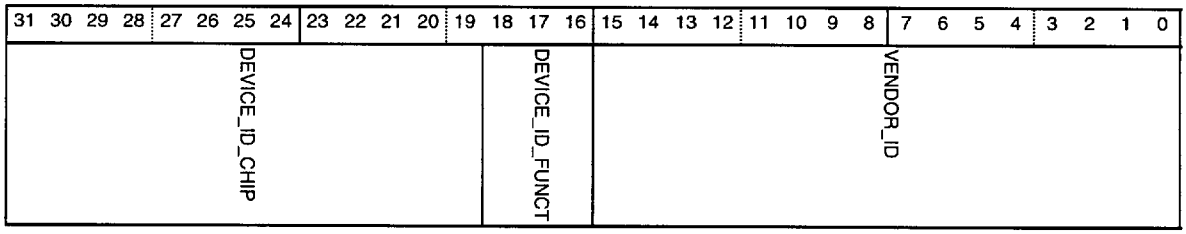
Descriptions of register contents include an indication if register fields are readable **(R)** *or writable* **(W)** *and the initial power-on or reset value of the field* **(I)**. *'-' indicates not readable / writable, X indicates an indeterminate value, hence* I=X *indicates register or field not reset.*

A PCI CONFIGURATION REGISTERS

This section describes the 256 byte PCI configuration spaces as implemented by the STG2000. Two PCI functions, NV and VGA, are defined by the STG2000 which decodes and acknowledges the first 512 bytes of the configuration address space. The STG2000 does not respond (does not assert **DEVSEL#**) for functions 2 - 7.

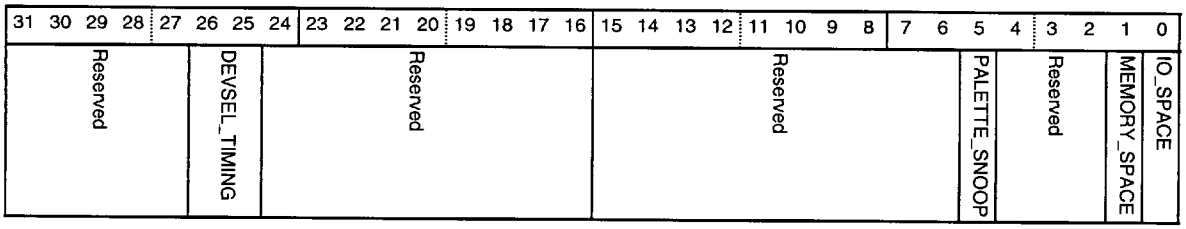
A.1 REGISTER DESCRIPTIONS FOR FUNCTION 0 (VGA)

PCI Configuration Register 0x00



Bits	Function	R W I
31:19	The DEVICE_ID_CHIP bits contain the chip number allocated by the manufacturer to identify the particular device. 1=STG2000	R - 1
18:16	The DEVICE_ID_FUNC bits contain the function number from the Configuration Address bits [10:8]. 0=VGA function	R - 1
15:0	VENDOR_ID bits allocated by the PCI Special Interest Group to uniquely identify the manufacturer of the device. 0x104A=SGS-THOMSON Microelectronics	R - X

PCI Configuration Register 0x04



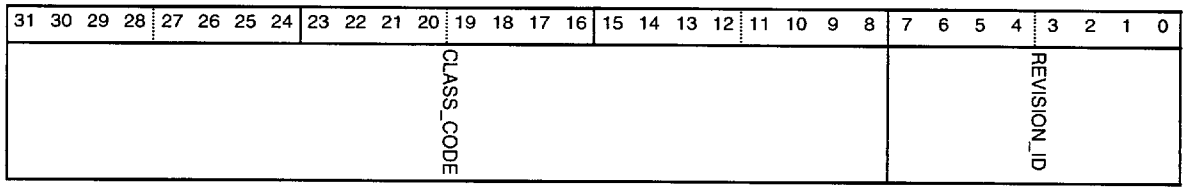
Device Status Field (bits [31:16])

Bits	Function	R W I
31:27	Reserved	R - 0
26:25	The DEVSEL_TIMING bits indicate the timing of **DEVSEL#**. These bits indicate the slowest time that the STG2000 asserts **DEVSEL#** for any bus command except Configuration Read and Configuration Write. The STG2000 responds with medium **DEVSEL#** for the VGA device. 01=medium	R - 1
24:16	Reserved	R - 0

Device Control Command Field (bits[15:0])

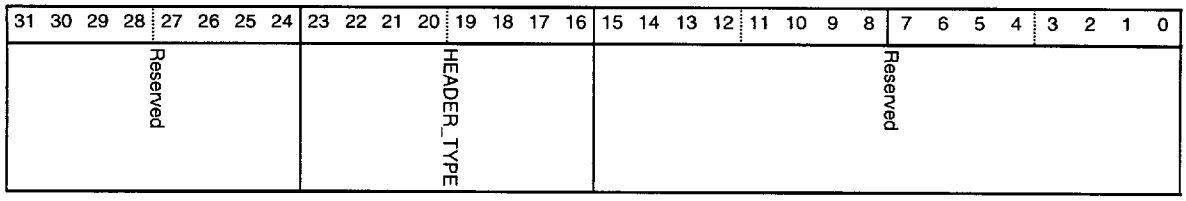
Bits	Function	R W I
15:6	Reserved	R - 0
5	PALETTE_SNOOP indicates that VGA compatible devices should snoop their palette registers. 0=Palette accesses treated like all other accesses 1=Enables special palette snooping behavior	R W 0
4:2	Reserved	R - 0
1	MEMORY_SPACE indicates that the STG2000 will respond to memory space accesses. 0=Device response disabled 1=Enables response to Memory space accesses.	R W 0
0	IO_SPACE indicates that the device will respond to I/O space accesses. For the VGA function this bit enables I/O space accesses.	R W 0

PCI Configuration Register 0x08



Bits	Function	R W I
31:8	The CLASS_CODE bits identify the generic function of the device and (in some cases) a specific register-level programming interface. The register is broken into three byte-size fields. The upper byte (at offset 0x0B) is a base class code which broadly classifies the type of function the device performs. The middle-byte (at offset 0x0A) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 0x09) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. The VGA function responds as a VGA compatible controller. 0x030000=VGA compatible controller	R - X
7:0	The REVISION_ID bits specify a device specific revision identifier. The value is chosen by the vendor. This field should be viewed as a vendor defined extension to the DEVICE_ID. 0x00=Rev A, 0x01=Rev B, 0x02=Rev C	R - X

PCI Configuration Register 0x0C



Bits	Function	R W I
31:24	Reserved	R - 0
23:16	HEADER_TYPE identifies the device as single or multi-function. STG2000 responds as a multi-function device. 0x80=Multiple function device	R - 0x80
16:00	Reserved	R - 0

PCI Configuration Register 0x10 — Base Memory Address Register

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
0x00000000							

Bits	Function	R W I
31:0	These bits are hardwired (read-only) to 0.	R - 0

PCI Configuration Registers 0x14 - 0x24 — Base Address Registers

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
0x00000000							

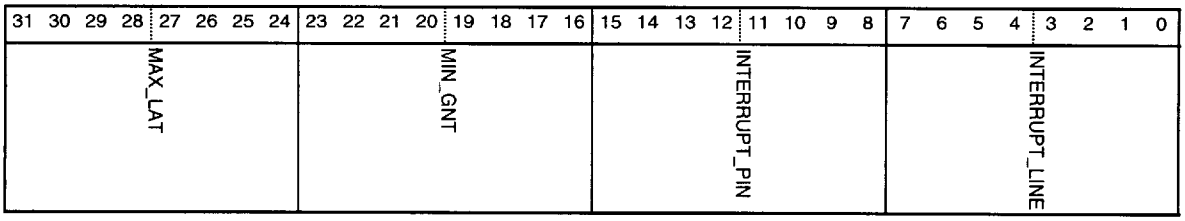
Bits	Function	R W I
31:0	These bits are hardwired (read-only) to 0.	R - 0

PCI Configuration Register 0x30 — Expansion ROM Base Address

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
ROM_BASE_ADDRESS				ROM_BASE_RESERVED		Reserved	ROM_DECODE

Bits	Function	R W I
31:22	The ROM_BASE_ADDR bits contain the base address of the Expansion ROM. The bits correspond to the upper bits of the Expansion ROM base address. This decode permits the PCI boot manager to place the expansion ROM on a 4MByte boundary. STG2000 currently maps a 32KByte BIOS into the bottom of this 4MByte range. The writable bits are aliased between the NV and VGA devices.	R W X
21:11	ROM_BASE_RESERVED contain the lower bits of the base address of the Expansion ROM. These bits are hardwired to 0, forcing a 4MByte boundary.	R - 0
10:1	Reserved	R - 0
0	The ROM_DECODE bit indicates whether or not the STG2000 accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled using the parameters in the other part of the base register. The MEMORY_SPACE bit (PCI Configuration Register 0x04, page 46) has precedence over the ROM_DECODE bit. STG2000 will respond to accesses to its expansion ROM only if both the MEMORY_SPACE bit and the ROM_DECODE bit are set to 1. 0=Expansion ROM address space is disabled 1=Expansion ROM address decoding is enabled	R W 0

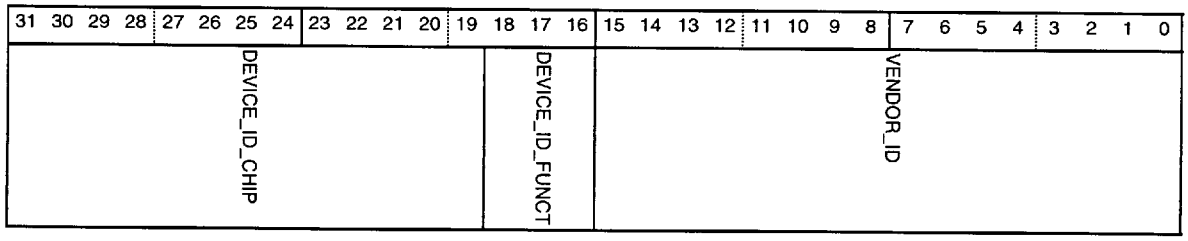
PCI Configuration Register 0x3C



Bits	Function	R W I
31:24	The MAX_LAT bits contain the maximum time the STG2000 requires to gain access to the PCI bus. This read-only register is used to specify the STG2000's desired settings for Latency Timer values. The value specifies a period of time in units of 250ns. 0=No requirements (VGA function)	R - 0
23:16	The MIN_GNT bits contain the length of the burst period the STG2000 needs, assuming a clock rate of 33MHz. This read-only register is used to specify the STG2000's desired settings for Latency Timer values. The value specifies a period of time in units of 250ns. 0=No requirements (VGA function)	R - 0
15:8	The INTERRUPT_PIN bits contain the interrupt pin the device (or device function) uses. A value of 1 corresponds to **INTA#**. The NV, VGA, and real mode devices all use **INTA#**.	R - 1
7:0	The INTERRUPT_LINE bits contain the interrupt routing information. POST software will write the routing information into this register as it initializes and configures the system. The value in this field indicates which input of the system interrupt controller(s) the STG2000's interrupt pin is connected to. Device drivers and operating systems can use this information to determine priority and vector information. INTERRUPT_LINE is initialized to 0xFF (no connection) at reset. 0=Interrupt line IRQ0 1=Interrupt line IRQ1 0xF=Interrupt line IRQ15 0xFF=No interrupt line connection (reset value)	R W 0xFF

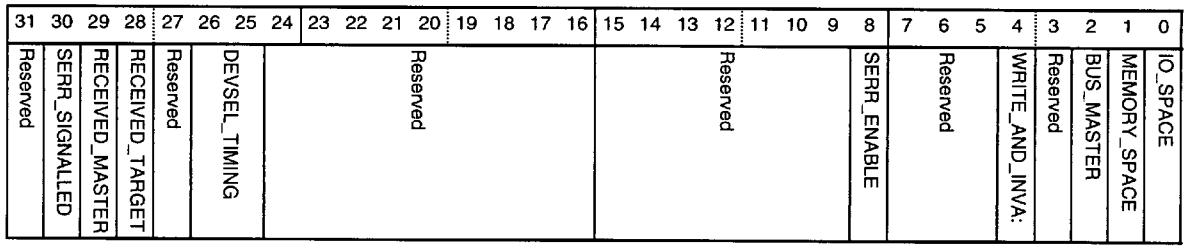
A.2 REGISTER DESCRIPTIONS FOR FUNCTION 1 (NV)

PCI Configuration Register 0x00



Bits	Function	R W I
31:19	The DEVICE_ID_CHIP bits contain the chip number allocated by the manufacturer to identify the particular device. 1=STG2000	R - 1
18:16	The DEVICE_ID_FUNC bits contain the function number from the Configuration Address bits [10:8]. 1=NV function	R - 0
15:0	VENDOR_ID bits allocated by the PCI Special Interest Group to uniquely identify the manufacturer of the device. 0x104A=SGS-THOMSON Microelectronics	R - X

PCI Configuration Register 0x04



Device Status Field (bits [31:16])

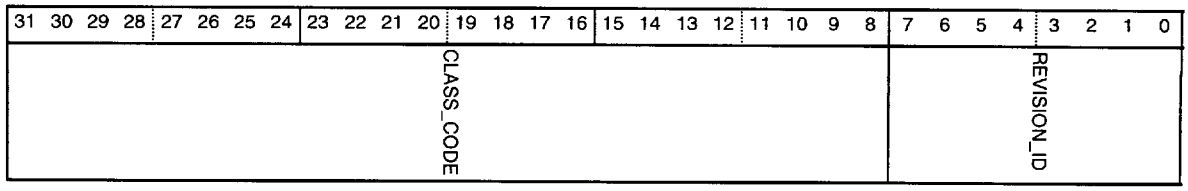
Bits	Function	R W I
31	Reserved	R - 0
30	SERR_SIGNALLED is set whenever the STG2000 asserts **SERR#**.	R W 0
29	RECEIVED_MASTER indicates that a master device's transaction (except for Special Cycle) was terminated with a master-abort. This bit is clearable (=1) in the NV device. 0=No abort 1=Master aborted	R W 0
28	RECEIVED_TARGET indicates that a master device's transaction was terminated with a target-abort. This bit is clearable (=1) in the NV device. 0=No abort 1=Master received target aborted	R W 0
27	Reserved	R - 0
26:25	The DEVSEL_TIMING bits indicate the timing of **DEVSEL#**. These bits indicate the slowest time that the STG2000 asserts **DEVSEL#** for any bus command except Configuration Read and Configuration Write. The STG2000 responds with fast **DEVSEL#** (0-cycle) except for retry accesses which respond with a medium **DEVSEL#**. 00=fast	R - 00
24:16	Reserved	R - X

Device Control Command Field (bits[15:0])

Bits	Function	R W I
15:9	Reserved	R - 0
8	SERR_ENABLE is an enable bit for the **SERR#** driver. 0=Disables the **SERR#** driver 1=Enables the **SERR#** driver	R W 0
7:5	Reserved	R W 0
4	WRITE_AND_INVAL is an enable bit for using the Memory Write and Invalidate command. 1=The STG2000 as bus master may generate the command 0=The Memory Write command must be used instead of Memory Write and Invalidate	R W 0
3	Reserved	R - 0

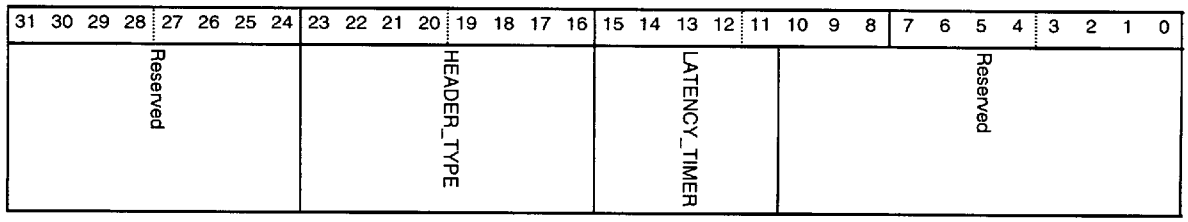
Bits	Function	R W I
2	BUS_MASTER indicates that the device can act as a master on the PCI bus. 0=Disables the STG2000 from generating PCI accesses 1=Allows the STG2000 to behave as a bus master	R W 0
1	MEMORY_SPACE indicates that the STG2000 will respond to memory space accesses. 0=Device response disabled 1=Enables response to Memory space accesses.	R W 0
0	IO_SPACE indicates that the device will respond to I/O space accesses. Although this bit is read/writable for the NV function, it is for reference only since the NV device has no I/O space.	R W 0

PCI Configuration Register 0x08



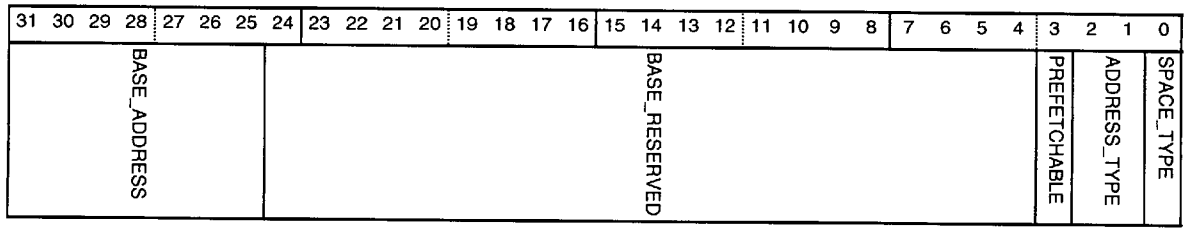
Bits	Function	R W I
31:8	The CLASS_CODE bits identify the generic function of the device and (in some cases) a specific register-level programming interface. The register is broken into three byte-size fields. The upper byte (at offset 0x0B) is a base class code which broadly classifies the type of function the device performs. The middle-byte (at offset 0x0A) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 0x09) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. The NV function responds as 0x048000 = 'Multifunction Device'.	R - 0x048000
7:0	The REVISION_ID bits specify a device specific revision identifier. The value is chosen by the vendor. This field should be viewed as a vendor defined extension to the DEVICE_ID. 0x00=Rev A, 0x01=Rev B, 0x02=Rev C	R - X

PCI Configuration Register 0x0C



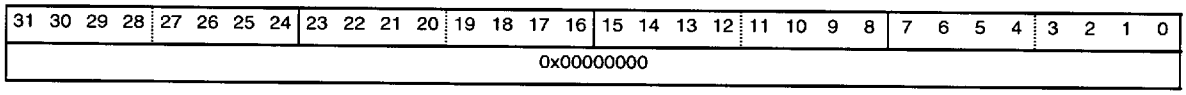
Bits	Function	R W I
31:24	Reserved	R - 0
23:16	HEADER_TYPE identifies the device as single or multi-function. STG2000 responds as a multi-function device. 0x80=Multiple function device	R - 0x80
15:11	The LATENCY_TIMER bits contain, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. 0=0 clocks, 1=8 clocks, 30=240 clocks, 31=248 clocks	R W 0
10:0	Reserved	R - 0

PCI Configuration Register 0x10 — Base Memory Address Register



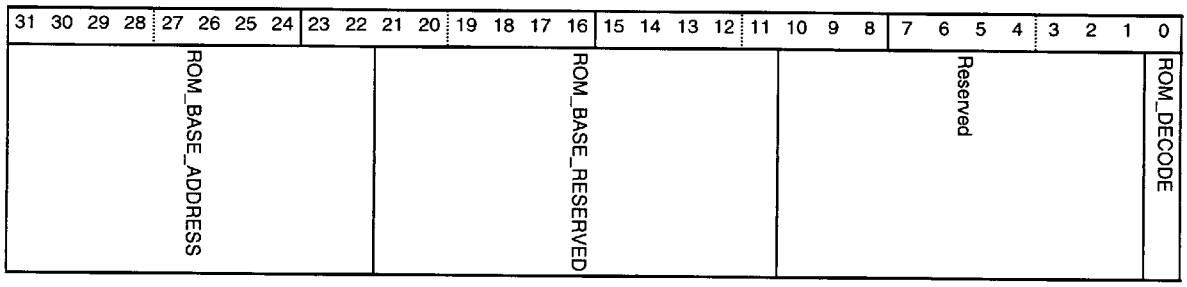
Bits	Function	R W I
31:25	The BASE_ADDRESS bits contain the most significant bits of the base address of the device. For the NV function this indicates that the STG2000 requires a 32MByte block of contiguous memory beginning on a 32MByte boundary.	R W 0
24:4	The BASE_RESERVED bits form the least significant bits of the base address and are hardwired to 0.	R - 0
3	The PREFETCHABLE bit indicates that there are no side effects on reads, that the device returns all bytes on reads regardless of the byte enables, and that host bridges can merge processor writes into this range without causing errors.	R - 1
2:1	The ADDRESS_TYPE bits contain the type (width) of the Base Address. 0=32-bit	R - 0
0	The SPACE_TYPE bit indicates whether the register maps into Memory or I/O space. 0=Memory space	R - 0

PCI Configuration Registers 0x14 - 0x24 — Base Address Registers



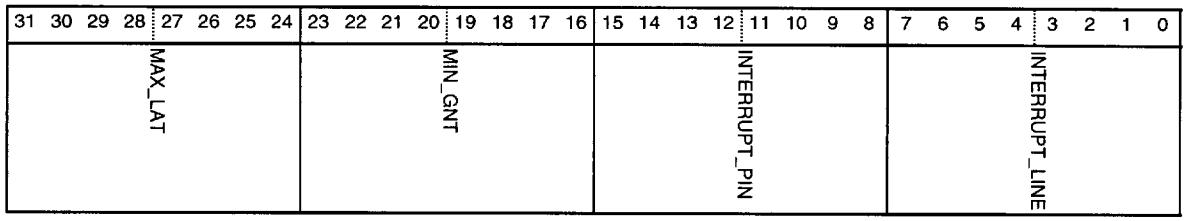
Bits	Function	R W I
31:0	These bits are hardwired (read-only) to 0.	R - 0

PCI Configuration Register 0x30 — Expansion ROM Base Address



Bits	Function	R W I
31:22	The ROM_BASE_ADDR bits contain the base address of the Expansion ROM. These bits correspond to the upper bits of the Expansion ROM base address. This decode permits the PCI boot manager to place the expansion ROM on a 4MByte boundary. STG2000 currently maps a 32KByte BIOS into the bottom of this 4MByte range. The writable bits are aliased between the NV and VGA devices.	R W X
21:11	ROM_BASE_RESERVED contain the lower bits of the base address of the Expansion ROM. These bits are hardwired to 0, forcing a 4MByte boundary.	R - 0
10:1	Reserved	R - 0
0	The ROM_DECODE bit indicates whether or not the STG2000 accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled using the parameters in the other part of the base register. The MEMORY_SPACE bit (PCI Configuration Register 0x04, page 52) has precedence over the ROM_DECODE bit. STG2000 will respond to accesses to its expansion ROM only if both the MEMORY_SPACE bit and the ROM_DECODE bit are set to 1. 0=Expansion ROM address space is disabled 1=Expansion ROM address decoding is enabled	R W 0

PCI Configuration Register 0x3C



Bits	Function	R W I
31:24	The MAX_LAT bits contain the maximum time the STG2000 requires to gain access to the PCI bus. This read-only register is used to specify the STG2000's desired settings for Latency Timer values. The value specifies a period of time in units of 250ns. 1=250ns (NV function)	R - 1
23:16	The MIN_GNT bits contain the length of the burst period the STG2000 needs, assuming a clock rate of 33MHz. This read-only register is used to specify the STG2000's desired settings for Latency Timer values. The value specifies a period of time in units of 250ns. 3=750ns (NV function)	R - 3
15:8	The INTERRUPT_PIN bits contain the interrupt pin the device (or device function) uses. A value of 1 corresponds to **INTA#**. The NV, VGA, and real mode devices all use **INTA#**.	R - 1
7:0	The INTERRUPT_LINE bits contain the interrupt routing information. POST software will write the routing information into this register as it initializes and configures the system. The value in this field indicates which input of the system interrupt controller(s) the STG2000's interrupt pin is connected to. Device drivers and operating systems can use this information to determine priority and vector information. INTERRUPT_LINE is initialized to 0xFF (no connection) at reset. 0=Interrupt line IRQ0 1=Interrupt line IRQ1 0xF=Interrupt line IRQ15 0xFF=No interrupt line connection (reset value)	R W 0xFF

B GAME PORT REGISTER

The STG2000 implements an IBM-compatible game port at I/O address 0x201. This supports four analog and four digital inputs for interfacing to joysticks and other devices used by games.

Game Port Register

0x201

7	6	5	4	3	2	1	0
DSD				ASD			

DSD Digital Switch Data (bits [7:4], R/*/I=X)

DSD=0 Closed (trigger pressed)

DSD=1 Open (trigger not pressed)

ASD Analog Switch Data (bits [3:0], R/*/I=X)

To determine the resistive value on an analog input, the time for the individual bits to flip from 1 to 0 must be measured. The analog bits [3:0] are set by a write to I/O location 0x201. The application must begin timing at this point and then poll until the bit corresponding to the required channel changes to a zero. The length of time for this to occur is proportional to the resistive value.

ASD=0 Timed out

ASD=1 Not timed out (waiting)

* Writing to this register will perform a reset as described above.

C MPU-401 REGISTERS

The STG2000 implements an MPU-401 (MIDI Processing Unit) compatible interface. It supports simple UART mode only. UART mode is set to simple when the value 0x3F is written to the MPU Command Port Register. The MPU-401 is reset by writing 0xFF to the MPU Command Port Register. The STG2000 supports MPU-401 base addresses of 0x230, 0x300 and 0x330.

Command Port Register

0x231, 0x301 or 0x331

7	6	5	4	3	2	1	0
MPU command							

MPU Command (bits [7:0], - W - =X)

0x3F=Set UART mode. Once UART mode is set, subsequent writes to this register are interpreted as data. The exception is 0xFF (reset) which must be written twice to ensure that the MPU-401 is in idle mode.

0xFF=Reset.

Commands are acknowledged by the Data Port Register returning 0xFE. Note that when in UART mode the first reset command (0xFF) is not acknowledged.

Status Register

0x231, 0x301 or 0x331

7	6	5	4	3	2	1	0
SRD	SWR	Status data					

SRD Read Status (bit 7, R - I=X)

SRD=0 Able to read data

SRD=1 Read buffer empty

SWR Write status (bit 6, R - I=X)

SWR=0 Able to write data

SWR=1 Write buffer full. The write buffer can become full by either a write to the Data Port Register or the Command Port Register.

Data Port Register

0x230, 0x300 or 0x330

7	6	5	4	3	2	1	0
DATA							

DATA MPU data (bits [7:0], R/W/I=X)

D VGA REGISTERS

D.1 GENERAL REGISTERS

Miscellaneous Output Register

Write - 0x3C2, Read - 0x3CC

7	6	5	4	3	2	1	0
VSP	HSP	PB	Reserved	CS		ER	IOA

VSP Vertical Sync Polarity (bit 7, R/W/I=X)

VSP=0 Positive sync polarity

VSP=1 Negative sync polarity, see Table 19

HSP Horizontal Sync Polarity (bit 6, R/W/I=X)

HSP=0 Positive sync polarity

HSP=1 Negative sync polarity, see Table 19

Table 19. Vertical size selection

Bits 7	Bits 6	Vertical size
0	0	Reserved
0	1	400 lines
1	0	350 lines
1	1	480 lines

PB Page bit (bit 5, R/W/I=X)

Selects the 64K page of memory when the system is in one of the odd or even modes. (These modes are used in display modes 0, 1, 2, 3 and 7).

PB=0 selects the low 64K page of memory

PB=1 selects the high 64K page of memory

CS Clock Select (bits [3:2] R/W/I=X)

Selects the Master Clock source according to Table 20.

Table 20. Clock source selection

Bits 3	Bits 2	Function
0	0	Selects 25MHz clock
0	1	Selects 28MHz clock
1	0	Non-VGA standard clock selection
1	1	Non-VGA standard clock selection

ER Enable RAM (bit 1, R/W/I=X)

Enable access of CPU to video memory

ER=0 Disable access of the video memory from the CPU

ER=1 Enable access of the video memory from the CPU

IOA Input/Output Address (bit 0, R/W/I=X)

Selects the CRT controller addresses to allow the monochrome adapter (MDA) to coreside with the color/graphics adapter (CGA). The write addresses to the Feature Control Register are affected in the same way.

IOA=0 sets the CRT controller addresses to 0x03Bx and the address for the Input Status Register 1 to 0x03BA.

IOA=1 sets CRT controller addresses to 0x03Dx and the Input Status Register 1 address to 0x03DA.

Feature Control Register

Write - 0x3BA (mono)/0x3DA (color), Read - 0x3CA

7	6	5	4	3	2	1	0
Reserved				VSS	Reserved		

VSS Vertical Sync Select (bit 3, R/W/I=X)

VSS=0 Normal vertical sync output

VSS=1 Vertical sync output is the logical OR of the vertical sync and the vertical display enable

Input Status Register 0

Read - 0x3C2

7	6	5	4	3	2	1	0
VRI	Reserved (=00)		SS	Reserved			

VRI Vertical Retrace Interrupt (bit 7, R/-/I=X)

Indicates the state of the Vertical Interrupt.

VRI=0 Vertical retrace is occurring (VBlank)

VRI=1 Vertical retrace not occurring (active display)

SS Switch Sense (bit 4, R/-/I=X)

Indicates the sense switch status.

SS=0 Sense switch is off

SS=1 Sense switch is on

Input Status Register 1

Read - 0x3BA (mono), 0xDA (color)

7	6	5	4	3	2	1	0
Reserved				VR	Reserved		DE

VR Vertical retrace (bit 3, R/-/I=X)

Indicates the status of vertical retrace.

VRI=0 Active display or horizontal blanking

VRI=1 Vertical retrace, video is blanked

DE Display Enable NOT (bit 0, R/-/I=X)

Indicates the status of horizontal or vertical retrace.

DE=0 Active display

DE=1 Horizontal or vertical retrace, video is blanked

D.2 SEQUENCER REGISTERS

Sequencer Address Register

0x3C4

7	6	5	4	3	2	1	0
Reserved					INDEX		

INDEX Sequencer address (index) (bits[2:0], R/W/I=X)

These bits contain the index (0x00 to 0x04) of the currently active sequencer data register.

Reset register

0x3C5, Index=0x00

7	6	5	4	3	2	1	0
Reserved						SR	SR

SR Synchronous Reset (bit 1, R/W/I=X)

Generates a synchronous reset. A synchronous reset preserves memory contents and must be used before changing the Clocking Mode Register in order to preserve memory contents.

SR=0 Generate and hold the system in a reset condition

SR=1 Release the reset if bit 0 is inactive

SR Synchronous Reset (bit 0, R/W/I=X)

Identical in operation to bit 1.

Clocking mode register

0x3C5, Index=0x01

7	6	5	4	3	2	1	0
Reserved		SO	S4	DC	SL	Reserved	8/9

SO Screen Off (bit 5, R/W/I=X)

SO=0 Screen is turned on

SO=1 Screen is turned off

S4 Shift Four (bit 4, R/W/I=X)

Controls how often the video serializers should be loaded

S4=0 Load the serializers every character clock cycle

S4=1 Load the serializers every forth character clock cycle

DC Dot clock (bit 3, R/W/I=X)

The dot clock is the basic VGA dot rate clock derived from the Master Clock (as selected by the CS bits of the Miscellaneous Output Register, page 61)

DC=0 Sets the dot clock to the same frequency as the Master Clock

DC=1 Selects the dot clock to run at the Master Clock frequency divided by 2

SL Shift Load (bit 2, R/W/I=X)

This bit is significant only if bit 4 (S4) =0. These two bits combined allow the serializers to be loaded every cycle, every other cycle or every fourth cycle of the character clock.

SL=0 Load the serializers every character clock cycle

SL=1 Load the serializers every other character clock cycle

8/9 8/9 Dot clocks (bit 0, R/W/I=X)

Selects 8 or 9 dots per character modes. The 9 dot mode is used for alphanumeric modes 0+, 1+, 2+, 3+, 7 and 7+ only. All other modes must use 8 dots per character clock. Also see the ELG (Enable Line Graphic) bit of the Attribute Mode Control Register, page 79.

8/9=0 The character clock is generated 8 dots wide

8/9=1 The character clock is generated 9 dots wide

Map Mask Register

0x3C5, Index=0x02

7	6	5	4	3	2	1	0
Reserved				EM3	EM2	EM1	EM0

EM[3:0] Enable Map (bits[3:0], R/W/I=X)

When set to 1, the Enable Map bits enable system access to the corresponding map (VGA display plane).

Character Map Select Register

0x3C5, Index=0x03

7	6	5	4	3	2	1	0
Reserved		CMAH	CMBH	CMA		CMB	

In alphanumeric modes, bit 3 of the attribute byte normally defines the foreground intensity. This bit can be redefined as a switch between character sets, allowing 512 displayable characters. To enable this feature the Extended Memory (EM) bit in the Memory Mode Register (Index 0x04) should be set to 1 and different values for Character Map A and Character Map B should be selected.

CMAH Character Map A Select (MSB) (bit 5, R/W/I=X)

This bit is the most significant bit of the CMA field (see below).

CMBH Character Map B Select (MSB) (bit 4, R/W/I=X)

This bit is the most significant bit of the CMB field (see below).

CMA Character Map A (bits[3:2], R/W/I=X)

In conjunction with bit 5 (CMAH) selects one of eight possible character sets when the character's attribute byte, bit 3=1.

CMB Character Map B (bits[1:0], R/W/I=X)

In conjunction with bit 4 (CMBH) selects one of eight possible character sets when the character's attribute byte, bit 3=0.

Memory Mode Register

0x3C5, Index=0x04

7	6	5	4	3	2	1	0
Reserved				C4	O/E	EM	Reserved

C4 Chain 4 (bit 3, R/W/I=X)

This bit controls whether the display planes are selected via the Read Map Select Register (0x3CF, Index 0x04) or if the display planes are selected by the low order A1 and A0 address bits.

C4=0 Display planes selected via the Read Map Select Register

C4=1 Display planes are selected by the low order A1 and A0 address bits.

O/E Odd/Even (bit 2, R/W/I=X)

Determines whether a display plane is addressed sequentially or whether odd addresses access display planes 1 and 3 and even addresses access display planes 0 and 2. The value of this bit should always complement that of the O/E field in the Mode Register (0x3CF, Index 0x05).

O/E=0 Enables the odd/even addressing mode

O/E=1 Sequential addressing mode

EM Extended Memory (bit 1, R/-/I=1)

This bit has a value of 1 and is read only.

EM=1 Extended memory is present. It indicates that VGA display memory is 256Kbytes.

D.3 CRT CONTROLLER REGISTERS

CRT Controller Address Register

0x3B4 (mono), 0x3D4 (color)

7	6	5	4	3	2	1	0
Reserved			INDEX				

INDEX CRT Controller Register Address (index) (bits[4:0], R/W/I=X)

These bits contain the index (0x00 to 0x18) of the currently active CRT controller data register (0x3B5/3D5).

Horizontal Total Register

0x3B5 (mono), 0x3D5 (color), Index=0x00

7	6	5	4	3	2	1	0
HT							

HT Horizontal Total (bits[7:0], R/W/I=X)

Programmed value = Total number of horizontal characters required -5.

Horizontal Display End Register

0x3B5 (mono), 0x3D5 (color), Index=0x01

7	6	5	4	3	2	1	0
HDE							

HDE Horizontal Display End (bits[7:0], R/W/I=X)

Programmed value = Number of displayed characters per line -1.

Start Horizontal Blanking Register

0x3B5 (mono), 0x3D5 (color), Index=0x02

7	6	5	4	3	2	1	0
SHB							

SHB Start Horizontal Blanking (bits[7:0], R/W/I=X)

Programmed value = Character count which determines the point at which the Horizontal Blank signal goes active relative to the start of active display.

End Horizontal Blanking

0x3B5 (mono), 0x3D5 (color), Index=0x03

7	6	5	4	3	2	1	0
Reserved	DES		EHB				

Reserved (bit 7)

This bit =1 for normal operation.

DES Display Enable Skew (bits[6:5], R/W/I=X)

These bits control the amount of skew in character clocks that the display enable signal is delayed.

EHB End Horizontal Blanking (bits[4:0], R/W/I=X)

This field determines the end of the horizontal blanking period. The most significant bit is located in the EHB field of the End Horizontal Retrace Register.

Start Horizontal Retrace Register

0x3B5 (mono), 0x3D5 (color), Index=0x04

7	6	5	4	3	2	1	0
SHR							

SHR Start Horizontal Retrace (bits[7:0], R/W/I=X)

These bits specify the character position where the horizontal retrace signal goes active.

End Horizontal Retrace Register

0x3B5 (mono), 0x3D5 (color), Index=0x05

7	6	5	4	3	2	1	0
EHB	HRD		EHR				

EHB End Horizontal Blanking (bit 7, R/W/I=X)

The most significant bit of the EHB field in the End Horizontal Blanking Register.

HRD Horizontal Retrace Delay (bits [6:5], R/W/I=X)

These bits control the skew of the horizontal retrace signal (from 0 to 3 character clock units).

EHR End Horizontal Retrace (bits [4:0], R/W/I=X)

This field is compared with the Start Horizontal Retrace Register to give a horizontal character count at which the horizontal retrace signal goes inactive. When the low-order five bits of the Start Horizontal Retrace Register equal the five bits in the EHR field, the retrace time will end.

Vertical Total Register

0x3B5 (mono), 0x3D5 (color), Index=0x06

7	6	5	4	3	2	1	0
VT							

VT Vertical Total (bits [7:0], R/W/I=X)

This register contains the 8 low-order bits of a 10-bit vertical total. The vertical total value is the number of horizontal raster scans on the display, including vertical retrace, minus 2. This value determines the period of the vertical retrace signal.

The two high-order bits of this field are located in the Overflow Register (Index 0x07).

Overflow Register

0x3B5 (mono), 0x3D5 (color), Index=0x07

7	6	5	4	3	2	1	0
VRS9	VDE9	VT9	LC8	VBS8	VRS8	VDE8	VT8

VRS9 Vertical Retrace Start Bit 9 (bit 7, R/W/I=X)

Bit 9 of the Vertical Retrace Start value. The 8 low-order bits are located in the Vertical Retrace Start Register (Index 0x10). Bit 8 of this value is located in bit 2 of this register (VRS8).

VDE9 Vertical Display End Bit 9 (bit 6, R/W/I=X)

Bit 9 of the Vertical Display End value. The 8 low-order bits are located in the Vertical Display End Register (Index 0x12). Bit 8 of this value is located in bit 1 of this register (VDE8).

VT9 Vertical Total Bit 9 (bit 5, R/W/I=X)

Bit 9 of the Vertical Total value. The 8 low-order bits are located in the Vertical Total Register (Index 0x06). Bit 8 of this value is located in bit 0 of this register (VT8).

LC8 Line Compare Bit 8 (bit 4, R/W/I=X)

Bit 8 of the Line Compare value. The 8 low-order bits are located in the Line Compare Register (Index 0x17).

VBS8 Start Vertical Blanking Bit 8 (bit 3, R/W/I=X)

Bit 8 of the Start Vertical Blanking value. The 8 low-order bits are located in the Start Vertical Blanking Register (Index 0x15).

VRS8 Vertical Retrace Start Bit 8 (bit 2, R/W/I=X)

Bit 8 of the Vertical Retrace Start value, see bit 7 (VRS9) above.

VDE8 Vertical Display Enable End Bit 8 (bit 1, R/W/I=X)

Bit 8 of the Vertical Display Enable End value, see bit 6 (VDE9) above.

VT8 Vertical Total Bit 8 (bit 0, R/W/I=X)

Bit 8 of the Vertical Total value, see bit 5 (VT9) above.

Preset Row Scan Register

0x3B5 (mono), 0x3D5 (color), Index=0x08

7	6	5	4	3	2	1	0
Reserved	BP		PRS				

BP Byte Panning (bits [6:5], R/W/I=X)

Specifies the number of bytes to pan during a multiple shift panning operation.

PRS Preset Row Scan (bits [4:0], R/W/I=X)

Specifies the row scan count for the top row of character on the screen. Normally the value in this field is 0 which displays the full vertical extent of the top row of characters.

Maximum Scan Line Register

0x3B5 (mono), 0x3D5 (color), Index=0x09

7	6	5	4	3	2	1	0
2T4	LC9	VBS9	MSL				

2T4 200 to 400 Line Conversion (bit 7, R/W/I=X)

Allows a 200-line mode to be displayed on 400 display lines.

2T4=0 Normal operation, 200-line mode displayed without conversion

2T4=1 Display 200 lines on 400-line display

LC9 Line Compare Bit 9 (bit 6, R/W/I=X)

Bit 9 of the Line Compare value. The 8 low-order bits are located in the Line Compare Register (Index 0x17). Bit 8 of this value is located in bit 4 of the Preset Row Scan Register (LC8).

VBS9 Start Vertical Blanking Bit 9 (bit 5, R/W/I=X)

Bit 9 of the Start Vertical Blanking value. The 8 low-order bits are located in the Start Vertical Blanking Register (Index 0x15). Bit 8 of this value is located in bit 3 of the Preset Row Scan Register (VBS8).

MSL Maximum Scan Line (bits [4:0], -/W/I=X)

Specifies the number of scan lines per character row. The value of this field is the maximum row scan number minus 1.

Cursor Start Register

0x3B5 (mono), 0x3D5 (color), Index=0x0A

7	6	5	4	3	2	1	0
Reserved		CD	Reserved	CS			

CD Cursor Disable (bit 5, R/W/I=X)

CD=0 Cursor on

CD=1 Cursor off

CS Cursor Start (bits [3:0], R/W/I=X)

Specifies the first scan line within a character box where the cursor begins.

Cursor End Register

0x3B5 (mono), 0x3D5 (color), Index=0x0B

7	6	5	4	3	2	1	0
Reserved	CSK		CE				

CSK Cursor Skew (bits [6:5], R/W/I=X)

Specifies the number of character clocks the cursor is shifted to the right.

CE Cursor end (bits [4:0], R/W/I=X)

Specifies the row within the character box where the cursor ends.

Start Address High Register

0x3B5 (mono), 0x3D5 (color), Index=0x0C

7	6	5	4	3	2	1	0
SAH							

SAH Start Address High (bits [7:0], R/W/I=X)

The high order byte of the 16-bit starting address pointing to the first address after vertical retrace of the display buffer.

Start Address Low Register

0x3B5 (mono), 0x3D5 (color), Index=0x0D

7	6	5	4	3	2	1	0
SAL							

SAL Start Address Low (bits [7:0], R/W/I=X)

The low order byte of the 16-bit starting address pointing to the first address after vertical retrace of the display buffer.

Cursor Location High Register

0x3B5 (mono), 0x3D5 (color), Index=0x0E

7	6	5	4	3	2	1	0
CLH							

CLH Cursor Location High (bits [7:0], R/W/I=X)

The high order byte of the 16-bit display buffer address defining the cursor location.

Cursor Location Low Register

0x3B5 (mono), 0x3D5 (color), Index=0x0F

7	6	5	4	3	2	1	0
CLL							

CLL Cursor Location Low (bits [7:0], R/W/I=X)

The low order byte of the 16-bit display buffer address defining the cursor location.

Vertical Retrace Start Register

0x3B5 (mono), 0x3D5 (color), Index=0x10

7	6	5	4	3	2	1	0
VRS							

VRS Vertical Retrace Start (bits [7:0], R/W/I=X)

The eight low-order bits of the 9-bit start position of the vertical retrace signal, programmed in horizontal scan lines. Bit 8 is in the Overflow Register (Index 0x07).

Vertical Retrace End Register

0x3B5 (mono), 0x3D5 (color), Index=0x11

7	6	5	4	3	2	1	0
PR	BW	DVI	CVI	EVR			

PR Protect Registers 0-7 (bit 7, R/W/I=X)

Protects CRT controller registers at indexes 0 - 7 from being modified.

PR=0 Enables write access to CRT controller registers

PR=1 Disables write access to CRT controller registers

BW Bandwidth (bit 6, R/W/I=X)

Selects three or five DRAM refresh cycles per horizontal line. This Read/Write location does not have any controlling function and is supported for compatibility only.

DVI Disable Vertical Interrupts (bit 5, R/W/I=X)

DVI=0 Enable vertical interrupts

DVI=1 Disable vertical interrupts

CVI Disable Vertical Interrupts (bit 4, R/W/I=X)

CVI=0 Clear vertical interrupts

CVI=1 No effect

EVR End Vertical Retrace (bits [3:0], R/W/I=X)

These four bits are compared with the value in the Vertical Retrace Start Register (Index 0x10) to determine when the vertical retrace period ends.

Vertical Display Enable End Register

0x3B5 (mono), 0x3D5 (color), Index=0x12

7	6	5	4	3	2	1	0
VDE							

VDE Vertical Display Enable End (bits [7:0]) R/W/I=X)

The eight low-order bits of a 10-bit value that determines the last horizontal scan line of the display. This value is equal to the total number of scan lines minus 1.

Offset Register

0x3B5 (mono), 0x3D5 (color), Index=0x13

7	6	5	4	3	2	1	0
OFF							

OFF Character Offset Pitch (bits [7:0], R/W/I=X)

This field determines the logical line width of the display. The offset value corresponds to the difference between the addresses of two vertically neighboring pixels.

Underline Location Register

0x3B5 (mono), 0x3D5 (color), Index=0x14

7	6	5	4	3	2	1	0
Reserved	DW	CB4	UL				

DW Doubleword Mode (bit 6, R/W/I=X)

Selects normal addressing or doubleword addressing.

DW=0 Normal word addressing

DW=1 Doubleword addressing

CB4 Count by Four (bit 5, R/W/I=X)

If doubleword addressing is enabled, this field controls the clock to the memory address counter.

CB4=0 Normal clocking

CB4=1 Divide the clock to the memory address counter by 4

UL Underline Location (bits [4:0], R/W/I=X)

The value in this field plus 1 determines the horizontal scan line within a character box on which the underline will occur.

Start Vertical Blank Register

0x3B5 (mono), 0x3D5 (color), Index=0x15

7	6	5	4	3	2	1	0
VBS							

VBS Vertical Blank Start (bits [7:0], R/W/I=X)

The low order 8 bits of the 9-bit value that is compared to the horizontal scan line counter (bit 8 is in the Overflow Register (Index 0x07). When these two values are equal, the vertical blanking period begins.

End Vertical Blank Register

0x3B5 (mono), 0x3D5 (color), Index=0x16

7	6	5	4	3	2	1	0
Reserved	VBE						

VBE Vertical Blank End (bits [6:0], R/W/I=X)

This 7-bit value is compared to the horizontal scan line counter. When these two values are equal, the vertical blanking period ends.

Mode Control Register

0x3B5 (mono), 0x3D5 (color), Index=0x17

7	6	5	4	3	2	1	0
HW	W/B	AW	Reserved	CBT	HRS	SRS	CMS

HW Hardware Reset (bit 7, R/W/I=X)

Enables or disables generation of the hardware horizontal and vertical retrace signals, display enable signals and blanking signals.

HW=0 Reset condition, timing signals disabled.

HW=1 Timing signals enabled.

W/B Word/Byte Mode (bit 6, R/W/I=X)

Controls the way display memory is addressed.

W/B=0 Word mode is selected. This mode shifts the memory address counter bits down one bit; the most significant bit of the counter appears on the least significant bit of the memory address outputs.

W/B=1 Byte mode is selected; addresses are output to the display memory without being shifted.

AW Address Wrap (bit 5, R/W/I=X)

Determines whether bit 13 or 15 should be output on the least significant address line to the display memory when the system is in word mode.

AW=0 Address bit 13 is selected as the least significant address bit to the display memory.

AW=1 Address bit 15 is selected as the least significant address bit to the display memory.

CBT Count By Two (bit 3, R/W/I=X)

This bit is used to create either a byte or word refresh address for the display buffer.

CBT=0 Address counter uses the character clock (byte address).

CBT=1 Address counter uses the character clock divided by two (word address).

HRS Horizontal Retrace Select (bit 2, R/W/I=X)

This bit selects the clock controlling the vertical timing counter to be either the horizontal retrace clock (HRS=0) or horizontal retrace clock divided by 2 (HRS=1).

Dividing the clock effectively doubles the vertical resolution of the CRT controller. The vertical counter has a maximum resolution of 1024 scan lines because the vertical total value is 10 bits wide. If the vertical counter is clocked with the horizontal retrace divided by 2, the vertical resolution is doubled to 2048 scan lines.

SRS Select Row Scan Counter (bit 1, R/W/I=X)

This bit selects the source of bit 14 of the output multiplexer. When set to 0, bit 1 of the row scan counter is the source. When set to 1, bit 14 of the address counter is the source.

CMS Compatibility Mode Support (bit 0, R/W/I=X)

The CMS bit selects the source of bit 13 of the output multiplexer. When set to 0, bit 0 of the row scan counter is the source. When set to 1, bit 13 of the address counter is the source.

Line Compare Register

0x3B5 (mono), 0x3D5 (color), Index=0x18

7	6	5	4	3	2	1	0
LC							

LC Line Compare (bits [7:0], R/W/I=X)

The 8 low order bits of the 10-bit Line Compare value. When the vertical counter reaches the Line Compare target value the internal address of the line counter is cleared. This creates a split screen where the lower screen is immune to scrolling. Bit 8 of this value is in the Overflow Register (page 67) and bit 9 in the Maximum Scan Line Register (page 68).

D.4 GRAPHICS CONTROLLER REGISTERS

Graphics Controller Address Register

0x3CE

7	6	5	4	3	2	1	0
Reserved				INDEX			

INDEX Graphics Controller Address (index) (bits[3:0], R/W/I=X)

This register is loaded with an index to the desired data register within the graphics controller. This index value is added to the graphics controller offset to access the data register.

Set/Reset Register

0x3CF, Index=0x00

7	6	5	4	3	2	1	0
Reserved				S/R			

S/R Set/Reset (bits [3:0], R/W/I=X)

These bits contain the value (0 or 1) written to the respective display plane when enabled by the Enable Set/Reset Register (Index 0x01).

Bit 0 = Value for display plane 0

Bit 1 = Value for display plane 1

Bit 2 = Value for display plane 2

Bit 3 = Value for display plane 3

Enable Set/Reset Register

0x3CF, Index=0x01

7	6	5	4	3	2	1	0
Reserved				ESR			

ESR Set/Reset (bits [3:0], R/W/I=X)

These bits enable the value contained in the Set/Reset Register (Index 0x00) to be written to the respective display plane. When a bit is set to 1, the respective display plane receives the value contained in the Set/Reset Register, when set to 0 that plane is written with data from the system (CPU).

Color Compare Register

0x3CF, Index=0x02

7	6	5	4	3	2	1	0
Reserved				CC			

CC Color Compare (bits [3:0], R/W/I=X)

The value in this field represents a 4-bit color. This color value, contained in bits 3 to 0, is compared with display planes 3 to 0 respectively. A mask for the color compare operation is contained in the Color Don't Care Register (Index 0x07).

Data Rotate Register

0x3CF, Index=0x03

7	6	5	4	3	2	1	0
Reserved			FS		DR		

FS Function Select (bits [4:3], R/W/I=X)

Data written from the host to the display memory may be modified according to a logic function performed with data already present in display memory. The function selected is determined as shown in Table 21.

Table 21. Function select operations

Bits 4	Bits 3	Function
0	0	Data is written unmodified
0	1	Data ANDed with latched data
1	0	Data ORed with latched data
1	1	Data XORed with latched data

DR Data Rotate (bits [2:0], R/W/I=X)

Data written from the host to display memory will be rotated to the right by the rotate count contained in this field. If a rotate operation is selected, it will be performed before the logical function selected in the FS field.

Read Map Select Register

0x3CF, Index=0x04

7	6	5	4	3	2	1	0
Reserved						RMS	

RMS Read Map Select (bits [1:0], R/W/I=X)

These bits select the display plane for system read operations.

Mode Register

0x3CF, Index=0x05

7	6	5	4	3	2	1	0
Reserved	SR		O/E	RM	Reserved	WM	

SR Shift Register (bits [6:5], R/W/I=X)

This field controls the formatting of data output from the display planes. Formatting of data for straight VGA addressing, CGA compatibility or VGA mode 0x13 (265 color) are selected as shown in Table 22.

Table 22. Formatting of data output

Bits 6	Bits 5	Function
0	0	Output the data with each display plane output on its associated serial output. This is the standard VGA format.
0	1	Output the data in a CGA compatible 320x200, four color graphics mode. This is used in display modes 0x04 and 0x05.
1	x	Output the data eight bits at a time from the four bit planes. This is the format for VGA mode 0x13.

O/E Odd/Even (bit 4, R/W/I=X)

This bit is used to select between the VGA or CGA compatible mode of operation. It should always be the complement of the O/E bit in the Memory Mode Register (0x3C5, Index=0x04).

OE=0 Normal operating VGA mode. Display planes are addressed sequentially.

OE=1 CGA compatible mode. Even host addresses access even display planes (0 and 2) and odd host addresses access odd display planes (1 and 3).

RM Read Mode (bit 3, R/W/I=X)

RM=0 Selects Read Mode 0. The system reads data from the display plane selected by the Read Map Select Register or selected by the two low order bits of the memory address (depending on the setting of the Chain 4 bit in the Memory Mode Register (0x3C5, Index=0x04)).

RM=1 Selects Read Mode 1. The system reads the results of the comparison of the four display planes and the Color Compare Register (Index 0x02).

WM Write Mode (bits [1:0], R/W/I=X)

This field selects Write Modes 0-3 as shown in Table 23.

Table 23. Write Modes 0-3

Bits 1	Bits 0	Function
0	0	Write Mode 0. The default mode. Each display plane is written with system data (if enabled by the Map Mask Register, page 64). If a count is specified in the Data Rotate Register (Index 0x03) the data is rotated. If the set/reset function is enabled for a specific plane, that plane receives the 8-bit value contained in the Set/Reset register.
0	1	Write Mode 1. This mode allows eight neighboring horizontal pixels in all four planes to be moved from one display memory location to another.
1	0	Write Mode 2. This mode writes to eight neighboring pixels in all four display planes simultaneously. Display plane *n* (0 through 3) is filled with 8 bits of the value (0 or 1) of data bit *n*.
1	1	Write Mode 3. Each display plane is written with the 8-bit value contained in the Set/Reset Register (Index 0x00) for that plane (the Enable Set/Reset Register has no effect). Rotated system data is ANDed with the Bit Mask Register (Index 0x08) to form an 8-bit value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

Miscellaneous Register

0x3CF, Index=0x06

7	6	5	4	3	2	1	0
Reserved				MM		COE	G/A

MM Memory Map (bits [3:2], R/W/I=X)

Display memory is mapped into the host processor's memory address space as shown in Table 24.

Table 24. Mapping of display memory

Bits 3	Bits 2	Function
0	0	0xA0000 - 0xAFFFF (64KByte)
0	1	0xA0000 - 0xAFFFF (64KByte), VGA modes 8-13
1	0	0xB0000 - 0xB0FFF (4KByte), VGA mode 7
1	1	0xB8000 - 0xBFFFF (32KByte), VGA modes 0-6

COE Chain Odd/Even (bit 1, R/W/I=X)

COE=0 Standard VGA addressing

COE=1 The host address bit 0 is replaced by a higher order address bit, causing even host addresses to access planes 0 and 2 and odd addresses to access planes 1 and 3. Used for MDA emulation.

G/A Graphics/Alphanumerics Mode (bit 0, R/W/I=X)

GA=0 Selects the alphanumeric operating mode

GA=1 Selects the graphics operating mode

Color Don't Care Register

0x3CF, Index=0x07

7	6	5	4	3	2	1	0
Reserved				CDC			

CDC Color Don't Care (bits [3:0], R/W/I=X)

Bits 0-3 contain mask bits for the respective display planes in the color comparison operation described for the Color Compare Register (Index 0x02). This register is used in Read Mode 1 only (as determined by the RM field of the Mode Register, page 75).

0= Plane does not participate in comparison operation.

1= Compare normal

Bit Mask Register

0x3CF, Index=0x08

7	6	5	4	3	2	1	0
BM							

BM Bit mask (bits [7:0], R/W/I=X)

This register applies to all display planes simultaneously. The eight bits of the BM field correspond to eight horizontal neighboring pixels.

BM=0 When a bit is set to 0, the corresponding bit position in each display plane is masked to prevent change.

BM=1 When a bit is set to 1, the corresponding bit position in each plane can be changed.

D.5 ATTRIBUTE CONTROLLER REGISTERS

Attribute Address Register

Write - 0x3C0, Read - 0x3C1

7	6	5	4	3	2	1	0
Reserved		PAS	INDEX				

The Attribute Address Register shares a common address with the indexed attribute register. Access to these registers is controlled by the setting of an internal flip-flop. If the state of the flip-flop = 0 the Attribute Address Register will be accessed, if the state = 1, the indexed attribute register will be accessed. The flip-flop state is cleared by reading the Input Status Register 1 (Read - 0x3BA (mono), 0x3DA (color)) and toggled following each write to the Attribute Address Register.

PAS Palette Address Source (bit 5, R/W/I=X)

This bit is set to zero when loading the attribute registers and set to 1 for normal operation.

INDEX Attribute controller address (index) (bits[4:0], R/W/I=X)

These bits contain the index (0x00 to 0x14) of the Attribute Controller data register required to be accessed.

Palette Registers 0 - F

Write - 0x3C1, Read - 0x3C1, Indexes=0x00 - 0x0F

7	6	5	4	3	2	1	0
Reserved		SR	SG	SB	R	G	B

The 6-bit Palette Registers allow dynamic mapping between the text attribute or graphic color input value and the display color on the CRT screen. The Palette registers should be modified only during vertical retrace to avoid unwanted effects on the displayed image.

SR Secondary Red (bit 5, R/W/I=X)

0=No secondary red, 1=secondary red present

SG Secondary Green (bit 4, R/W/I=X)

0=No secondary green, 1=secondary green present

SB Secondary Blue (bit 3, R/W/I=X)

0=No secondary blue, 1=secondary blue present

R Red (bit 2, R/W/I=X)

0=No red, 1= red present

G Green (bit 1, R/W/I=X)

0=No green, 1=green present

B Blue (bit 0, R/W/I=X)

0=No blue, 1=blue present

Attribute Mode Control Register

Write - 0x3C1, Read - 0x3C1, Index=0x10

7	6	5	4	3	2	1	0
IPS	PCS	PPC	Reserved	B/I	ELG	Reserved	

IPS Internal Palette Size (bit 7, R/W/I=X)

This bit selects the source of video bits [5:4] that act as inputs to the video DAC.

IPS=0 Video bits [5:4] are the outputs of the Palette Registers (Indexes 0x00 - 0x0F, see above).

IPS=1 Video bits [5:4] are bits [1:0] of the Color Select Register (Index 0x14)

PCS Pixel Clock Select (bit 6, R/W/I=X)

Allows selection of 256 colors in mode 0x13.

PCS=0 Normal operation

PCS=1 The video data is sampled so that 8 bits are available in the 256 color mode (0x13)

PPC Pixel Panning Compatibility (bit 5, R/W/I=X)

This bit allows a section of the screen to be panned independently during split screen operation.

PPC=0 Normal operation, line compare has no effect on the output of the Pixel Panning Register.

PPC=1 Top screen panning enabled in split screen mode. Line compare modifies output of the Pixel Panning Register.

B/I Enable Blink or Intensity (bit 3, -/W/I=X)

B/I=0 The most significant bit of the attribute byte selects the background intensity.

B/I=1 Enables blinking

ELG Enable Line Graphics Character Code (bit 2, -/R/I=0)

ELG=0 Set the ninth dot of the character to the background color, regardless of the character code.

ELG=1 Set the ninth dot of the character to the same value as the eighth dot for all graphics line characters (to support special line-character codes 0xC0 - 0x0F).

Overscan Color Register

Write - 0x3C0, Read - 0x3C1, Index=0x11

7	6	5	4	3	2	1	0
OC							

OC Overscan Color (bits [7:0], R/W/I=X)

Selects the color of the border (overscan) region of the display. Bits [7:0] address the Palette-DAC look-up table to select an 8-bit indexed color (1 of 256 colors from the standard palette).

Color Plane Enable Register

Write - 0x3C0, Read - 0x3C1, Index=0x12

7	6	5	4	3	2	1	0
Reserved				CPE			

CPE Color Planes Enable (bits [3:0], R/W/I=X)

The display planes may be selected or deselected depending on the values in this field. If a bit is set to 1, the respective plane is selected. Any combination of planes can be selected simultaneously.

Horizontal Pixel Panning Register

Write - 0x3C0, Read - 0x3C1, Index=0x13

7	6	5	4	3	2	1	0
Reserved				HPP			

HPP Horizontal Pixel Pan (bits [3:0], R/W/I=X)

Specifies the number of pixels to shift the video data to the left as shown in Table 25. It is used in conjunction with the starting address for smooth panning operations.

Table 25. Horizontal pixel panning (number of pixels shifted to the left)

Register value (HPP)	Mode 13	Alphanumeric modes	All other modes
0	0	1	0
1	-	2	1
2	1	3	2
3	-	4	3
4	2	5	4
5	-	6	5
6	3	7	6
7	-	8	7
8	-	0	-

Color Select Register

Write - 0x3C0, Read - 0x3C1, Index=0x14

7	6	5	4	3	2	1	0
Reserved				C67		C45	

C67 Color Register Address Bits 6 and 7 (bits [3:2], R/W/I=X)

Address bits 6 and 7 are combined with the six bits from the color palette to form the 8-bit address to the Palette-DAC.

C45 Color Register Address Bits 4 and 5 (bits [1:0]], R/W/I=X)

Address bits 4 and 5 are combined with the two bits in the C67 field and the four low order bits from the color palette to form the 8-bit address to the Palette-DAC. This field is only used if the IPS field of the Mode Control Register is set to 1.